STIC Search Report
EIC 2800

STIC Database Tracking Number: 97184

TO: William C Vesperman **Location: CP4 4D32** **Art Unit : 2813** **Wednesday, June 25, 2003** **Case Serial Number: 10/043237**	**From: Irina Speckhard** **Location: EIC 2800** **CP4-9C18** **Phone: 308-6559** **irina.speckhard@uspto.gov**

Search Notes

Examiner Vesperman,

Please find attached first-pass prior-art search results from the patent and non-patent abstract databases. The results were based on claims and statements of technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you need further searching or have questions or comments, please let me know.

Thank you,

Irina Speckhard

Case Serial Number 10/043237

25jun03 09:33:26 User267149 Session D790.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2003/Jun W3
(c) 2003 Institution of Electrical Engineers
*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 6:NTIS 1964-2003/Jun W4
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*File 6: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 8:Ei Compendex(R) 1970-2003/Jun W3
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*File 8: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 34:SciSearch(R) Cited Ref Sci 1990-2003/Jun W4
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File 35:Dissertation Abs Online 1861-2003/May
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File 65:Inside Conferences 1993-2003/Jun W4
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File 94:JICST-EPlus 1985-2003/Jun W4
(c)2003 Japan Science and Tech Corp(JST)
File 99:Wilson Appl. Sci & Tech Abs 1983-2003/May
(c) 2003 The HW Wilson Co.
File 144:Pascal 1973-2003/Jun W2
(c) 2003 INIST/CNRS
File 305:Analytical Abstracts 1980-2003/Jun W1
(c) 2003 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2003/May
(c) 2003 DECHEMA
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200340
(c) 2003 Thomson Derwent
File 347:JAPIO Oct 1976-2003/Feb(Updated 030603)
(c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2003/Mar
(c) 2003 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	2054	ANGLE??????(3N)IMPLANT????????
S2	569148	IMPLANT????????
S3	192189	ION(3N)IMPLANT????????
S4	569148	S1:S3
S5	1355338	IMPURIT???????? OR DOPA???????? OR DOPE??? OR DOPING
S6	165580	(FIELD()EFFECT? ?(1W)TRANSIT???????) OR FET? ?
S7	2492729	SEMICONDUCT???????
S8	470698	(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER?????)
S9	13123	(ETCH???????? OR CUT)(3N)CONDUCT????????
S10	1806677	(DIELECTRIC? OR OXIDE OR INSULAT? OR THIN)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER?????)
S11	17657	GATE?????(3N)(LONG???? OR LENGTH)
S12	1821421	S10:S11
S13	75416	(SOURCE OR DRAIN)(3N)(REGION? ? OR AREA? ?)
S14	2758	MASK??????(3N)(WIDE?? OR WIDTH)
S15	86248	S4 AND S5
S16	2816	S15 AND S6
S17	14793	(TAPER??????? OR NARROW????? OR THIN??????)(3N)GATE????
S18	87	S16 AND S17
S19	73	S18 AND S7
S20	36	S19 AND S8
S21	0	S20 AND S9
S22	33	S20 AND S12
S23	33	RD (unique items)
S24	3	S20 NOT S23
S25	3	RD (unique items)
S26	37	S19 NOT S20
S27	21	S26 AND S13
S28	21	S27 AND S13
S29	0	S28 AND S14
S30	20	RD S28 (unique items)
S31	86248	S4 AND S15
S32	62029	S31 AND S3
S33	2081	S32 AND S6
S34	2	S33 AND TAPER???(3N)GATE????
S35	2	RD (unique items)

35/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04312466
MANUFACTURE OF HIGH BREAKDOWN-STRENGTH MOS TYPE **FET**

PUB. NO.: 05-304166 [JP 5304166 A]
PUBLISHED: November 16, 1993 (19931116)
INVENTOR(s): KOBAYASHI KAZUO
APPLICANT(s): NEW JAPAN RADIO CO LTD [326320] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-166150 [JP 91166150]
FILED: June 12, 1991 (19910612)
JOURNAL: Section: E, Section No. 1512, Vol. 18, No. 105, Pg. 7, February 21, 1994 (19940221)

ABSTRACT

PURPOSE: To obtain a thick oxide film, by which field strength in the vicinity of a drain is reduced and breakdown strength is increased, on the drain side by leaving a taper-etched field oxide film at a position held by a low-**doped** drain region on the drain side and a polysilicon gate.

CONSTITUTION: The surface of a silicon substrate 1 is oxidized, opening sections for the diffusion of a channel stop and for the diffusion of a low-**doped** drain are formed, and a channel stop region and a low-**doped** drain region 2a are formed through a diffusion or **ion implantation**. A field oxide film 4 is shaped by a CVD oxide film, the oxide film having a shape having a smooth tapered angle is left on the section on the gate side of the low-**doped** drain region 2a and the oxide film 4 in an element forming region is removed through **taper** etching, a **gate** oxide film 5 is formed, polysilicon is deposited on the gate oxide film 5 and a polysilicon gate 6 is formed. Accordingly, the increase of breakdown strength can be realized without augmenting manhours and having an effect on the state of a low-**doped** drain layer.

35/3,AB/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03331728
MOS-**FET** AND MANUFACTURE THEREOF

PUB. NO.: 02-307228 [JP 2307228 A]
PUBLISHED: December 20, 1990 (19901220)
INVENTOR(s): MINAMI FUYUMI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-129329 [JP 89129329]
FILED: May 23, 1989 (19890523)
JOURNAL: Section: E, Section No. 1042, Vol. 15, No. 98, Pg. 82, March 08, 1991 (19910308)

ABSTRACT

PURPOSE: To reduce a resistance between source, drain and a gate electrode and to improve transistor characteristics by forming the side face shape of an upper half of a polysilicon layer of the **gate** electrode in a **tapered** shape extending from its upper part toward its lower part, and forming a high melting point metal layer in the same width as that of the upper part of the polysilicon layer.

CONSTITUTION: In a MOS-PET provided with a gate electrode 4 of a 2-layer structure having a polysilicon layer 6 and a high melting point metal layer 5 covering the upper part on a gate oxide film 3 covering an element region, the side shape of the upper part of the layer 6 is formed in a tapered state extending from the upper part toward the lower part, while the layer 5 is formed in the same width as that of the upper part of the layer 6. Thus, with the gate electrode as a mask predetermined **impurity** ions are **implanted** . Then, source and drain of LDD structure in which two **impurity** diffused regions having different junction depths and **impurity** concentrations are continuously formed are composed, and the source and the drain are superposed with the gate electrode.

23/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015279548
WPI Acc No: 2003-340479/200332
XRAM Acc No: C03-089207
XRPX Acc No: N03-272317
Semiconductor device, e.g. metal insulator **semiconductor** field effect transistor, includes element-forming **layer**, gate **insulating film**, gate **electrode**, and source and drain regions, formed on buried **insulating film**
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: FUJIWARA M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6501133	B1	20021231	US 200261320	A	20020204	200332	B

Priority Applications (No Type Date): JP 2001367945 A 20011130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6501133	B1		13	H01L-027/01	

Abstract (Basic): US 6501133 B1
Abstract (Basic):
NOVELTY - A **semiconductor** device comprises sequential element-forming **layer**, gate insulating **film** (5), a gate **electrode** (6), and source and drain regions (9), formed on a buried **insulating film** (2) of a **semiconductor** substrate (1).
DETAILED DESCRIPTION - A **semiconductor** device comprises sequential element-forming **layer**, gate insulating **film**, a gate **electrode**, and source and drain regions, formed on a buried **insulating film** of a **semiconductor** substrate. The source and drain regions are located on two sides of the gate electrode, respectively. The buried **insulating film** has a first part and a second part. The first part is located below the source and drain regions, and the second part is located below the **gate** electrode **thinner** than the first part. The source and drain regions have bottoms which contact the first part of the buried **insulating film**.
USE - As a **semiconductor** device, e.g. metal insulator **semiconductor FET**.
ADVANTAGE - The invention eliminates defects caused by **ion implantation**, thus providing a buried **insulating film** of high quality.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the **semiconductor** device.
Substrate (1)
Buried **insulating film** (2)
Gate **insulating film** (5)
Gate electrode (6)
Sidewall **insulating film** (8)
Source and drain regions (9)
pp; 13 DwgNo 1/20

23/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014583910
WPI Acc No: 2002-404614/200243
XRAM Acc No: C02-113657
XRPX Acc No: N02-317615
Fabrication of integrated circuits structure for **semiconductor** devices, e.g. metal oxide **semiconductor** field effect transistors, involves **implanting ion** at tilt **angle** non-orthogonal to plane of **semiconductor** layer
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N); MOULI C V (MOUL-I); ROBERTS C (ROBE-I)
Inventor: MOULI C V; ROBERTS C
Number of Countries: 096 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200219431	A2	20020307	WO 2001US26342	A	20010823	200243	B
US 20020050621	A1	20020502	US 2000648044	A	20000825	200243	
			US 200134778	A	20011227		
AU 200186666	A	20020313	AU 200186666	A	20010823	200249	
EP 1312110	A2	20030521	EP 2001966127	A	20010823	200334	
			WO 2001US26342	A	20010823		

Priority Applications (No Type Date): US 2000648044 A 20000825; US 200134778 A 20011227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200219431	A2	E	26	H01L-029/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

US 20020050621	A1	H01L-031/119	Div ex application US 2000648044	
AU 200186666	A	H01L-029/00	Based on patent WO 200219431	
EP 1312110	A2 E	H01L-021/336	Based on patent WO 200219431	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): WO 200219431 A2
Abstract (Basic):
NOVELTY - Integrated circuit structure is formed on a **semiconductor** layer by **implanting** ions into an **oxide layer** at an overlap region beneath the gate structure and adjacent a defined leading edge to a predetermined **ion implant** concentration. Ions are **implanted** at a tilt **angle** non-orthogonal to plane of **semiconductor** layer.
DETAILED DESCRIPTION - Fabrication of integrated circuit structure on a **semiconductor layer** involves forming an **oxide layer** on a **semiconductor layer** and a polysilicon **layer** on the **oxide layer**. The polysilicon **layer** is patterned into a gate structure (15) having a defined leading edge (17), and to expose the **oxide layer** (14). Ions are **implanted** into the **oxide layer** at an overlap region

(26) beneath the gate structure and adjacent the defined leading edge to a predetermined **ion implant** concentration to increase the electrical gate oxide thickness only in the overlap region without thickness growth of the **oxide layer**. Ions are **implanted** at a tilt **angle** non-orthogonal to the plane of the **semiconductor** layer.

USE - For fabrication of integrated circuit structure used in **semiconductor** devices, e.g. metal oxide **semiconductor** field effect transistors (MOSFETs), CMOS **FET** devices, dynamic random access memory (DRAM), static RAM, erasable programmable read-only memory, or application specific integrated circuits.

ADVANTAGE - Reduces Gate Induced Drain Leakage (GIDL) current of **FETs**. It can provide scaled-down **semiconductor** device having a **thinner gate** oxide with improved electrical performance, that is cost effective and manufacturable, which can be easily integrated into an existing process flow, and which does not increase the cycle time of the process flow.

DESCRIPTION OF DRAWING(S) - The drawing shows process steps in fabricating a gate structure.

oxide layer (14)
gate structure (15)
leading edge (17)
overlap region (26)
pp; 26 DwgNo 2C/3

23/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012851003
WPI Acc No: 2000-022835/200002
Related WPI Acc No: 1998-168422
XRAM Acc No: C00-005476
XRPX Acc No: N00-017000
Semiconductor device, e.g. static random access memory (SRAM)
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)
Inventor: SUNDARESAN R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5990528	A	19991123	US 96661252	A	19960610	200002 B
			US 97977192	A	19971124	

Priority Applications (No Type Date): US 96661252 A 19960610; US 97977192 A 19971124
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5990528	A		9	H01L-029/78	Div ex application US 96661252 Div ex patent US 5721163

Abstract (Basic): US 5990528 A
Abstract (Basic):
NOVELTY - A first channel region and part of second and third regions overlap a gate electrode. The first channel region forms the channel of a **thin film FET**. The first region has shorter width than the gate electrode. The second and third regions serve as a source and a drain of the **thin film FET** respectively.

DETAILED DESCRIPTION - A **semiconductor** device, including a **thin film FET** with a gate electrode, and a buried contact formed on a first **insulating layer** above a **doped semiconductor** substrate (10) of a first conductivity type comprising (P-):

(a) source/drain regions (12) of a **FET** formed in the substrate;

(b) first insulating **layer** (16) including a **dielectric layer** having a uniform thickness of 500-1000 Angstrom over the substrate;

(c) buried contact via opening (17) through the first **insulating layer** to the source/drain regions;

(d) **thin film FET** formed on the first **insulating layer**;

(e) single **conductor layer** (24) providing both a combined buried contact (BC) and **gate electrode** for the **thin film FET** including the gate electrode (24) formed on the first **insulating layer**, formed from titanium nitride or a refractory metal silicide;

(f) gate **oxide dielectric layer**, of uniform thickness, covering an upper surface and first and second side surfaces of the gate electrode;

(g) **doped** polycrystalline silicon **semiconductor** film formed over the first **insulating layer** and the gate

oxide, dielectric **layer** and the gate **electrode** having a Vt threshold **implant** provided by **dopant** of a second conductivity type (N) opposite from the first conductivity type (P-);

(h) first channel region of the second conductivity type (N) formed in the **doped** polycrystalline silicon film, having first and second ends;

(i) second region of the first conductivity type (P) formed in the **doped** polycrystalline silicon film, and in contact with the first end of the first channel region; and

(j) third region of the second conductivity type (N) formed in the **semiconductor** film in contact with the second end of the first channel region.

The first channel region and part of the second and third regions overlap the gate electrode. The first channel region forms the channel of the **thin film FET**. The first region has shorter width than the gate electrode. The second and third regions serve as a source and a drain of the **thin film FET** respectively.

An INDEPENDENT CLAIM is also included for an SRAM as above.

USE - Used as an SRAM (claimed).

ADVANTAGE - The problem of high negative threshold voltage is avoided.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of the above device.

doped semiconductor substrate (10)
source/drain regions (12)
first **insulating layer** (16)
buried contact via opening (17)
single **conductor layer** (24)
pp; 9 DwgNo 2/3

23/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012651084
WPI Acc No: 1999-457189/199938
XRAM Acc No: C99-134160
XRPX Acc No: N99-341893
Manufacture of field effect transistors having reduced source /drain and gate electrode resistance
Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)
Inventor: TSENG H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5933741	A	19990803	US 97912534	A	19970818	199938	B

Priority Applications (No Type Date): US 97912534 A 19970818
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5933741	A		9	H01L-021/336	

Abstract (Basic): US 5933741 A
Abstract (Basic):
NOVELTY - The transistors have self aligned metal silicide source/drains and tungsten silicide gate electrodes.
DETAILED DESCRIPTION - The method comprises providing a **semiconductor** substrate having field oxide isolation regions surrounding and electrically isolating device areas, and having a gate oxide formed by thermal oxidation on the device areas and covered by a **conductively doped** polysilicon **layer**. A silicon rich tungsten silicide layer is deposited on the polysilicon layer and these layers are patterned by photoresist masking and anisotropic etching leaving portions over the device areas to form gate electrodes. Lightly **doped** source/drain areas are formed adjacent to the gate electrodes by **ion implantation**, and a conformal **insulating layer** is deposited over the gate electrodes and elsewhere on the substrate. The **insulating layer** is anisotropically etched back to form sidewall **spacers** on the gate **electrodes**, and the structure thermally oxidised to form silicon oxide on the tungsten silicide gate electrodes and concurrently growing a thinner silicon oxide on the lightly **doped** source/drain areas. The thinner oxide is completely removed by plasma etching while concurrently retaining a portion of the oxide on the tungsten silicide gate **electrodes**. A blanket metal **layer** is deposited and the substrate annealed to form metal silicide on the source/drain areas while leaving unreacted metal on insulated surfaces. The unreacted metal is removed, and heavily **doped** source/drain areas are formed adjacent to the sidewall spacers by **ion implantation**.
USE - A method for making field effect transistors (**FETs**) having titanium silicide source/drain areas and tungsten silicide **FET** gate electrodes.
ADVANTAGE - A self aligned silicide process that reduces source/drain and gate resistance thereby improving device performance, and avoiding source/drain-to-gate bridging which causes electrical shorts.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional

view of the transistor.
Substrate (10)
Field oxide isolation region (12)
Thin gate oxide (14)
Polysilicon layer (16)
Tungsten silicide layer (18)
Source/drain areas (20)
Thick silicon **oxide layer** (24)
Titanium silicide layer (30)
heavily **doped** source/drain area (32)
Interlayer dielectric (34)
Electroconductive layer (36)
pp; 9 DwgNo 8/8

23/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011799604
WPI Acc No: 1998-216514/199819
XRAM Acc No: C98-068620
XRPX Acc No: N98-171195
Self-aligned silicide **narrow gate** electrodes preparation for **FET** manufacture - includes etching back **insulating layer** to silicon nitride layer to form self-aligned mask which prevents **implant** damage to shallow source/drain regions near the gate electrodes
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N); CHARTERED SEMICONDUCTOR MFG PTE LTD (CHAR-N)
Inventor: CHEN L; PEY K L; WONG H; CHAN L
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5731239	A	19980324	US 97787193	A	19970122	199819	B
SG 64468	A1	19990427	SG 9843	A	19980106	199933	

Priority Applications (No Type Date): US 97787193 A 19970122
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5731239	A		11	H01L-021/336	
SG 64468	A1			H01L-021/336	

Abstract (Basic): US 5731239 A

Field effect transistors (**FETs**) having low sheet resistance electrodes are manufactured by forming shallow trench isolation regions surrounding and electrically isolating device areas on a **semiconductor** substrate. A gate oxide is then formed over the device areas by thermal oxidation and a N+ **conductively doped** polysilicon **layer** is deposited on the substrate followed by a silicon nitride layer (18). The nitride and polysilicon layers are then patterned by photoresist masking and anisotropic etching to leave areas over the device areas to form the gate electrodes (16) and to form electrical interconnections over the shallow trench isolation regions. Lightly **doped** source/drain areas (24) are then **ion implanted** into areas next to the gate electrodes and a conformal **insulating layer** is deposited over the gate electrodes and other areas of the substrate. The **insulating layer** is etched back to form side-wall **spacers** on the gate **electrodes** and source/drain contact layers are formed next to them by **ion implantation**. A titanium blanket layer (30) is deposited and annealed to form titanium silicide (30') on the source/drain areas and unreacted titanium on the insulated areas which is stripped off. Another blanket **insulating layer** (28) is then deposited followed by chemical/mechanical polishing of the second **insulating layer** to the nitride **layer** on the gate **electrodes**. The silicon **layer** is then selectively wet etched away while leaving the second **insulating layer** as a self-aligning **implant** mask. Ions are then **implanted** in the polysilicon **layer** gate **electrodes**, while masking the source drain contact areas protected by the second **insulating layer**, which amorphises

the surface of the polysilicon layer. A second titanium layer is then deposited and annealed. Another method is also claimed.

ADVANTAGE - Sub-quarter micron wide gate electrodes having low sheet resistance are obtained using a pre-amorphisation **ion implantation** while avoiding **implant** damage to the source/drain areas. Costs are reduced due to the reduced number of photoresist masking steps necessary.

Dwg.5/9

23/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011751512
WPI Acc No: 1998-168422/199815
Related WPI Acc No: 2000-022835
XRAM Acc No: C98-053906
XRPX Acc No: N98-133764
Formation of SRAM including **thin film FET** and buried contact - using control gate electrode material having threshold level near intrinsic level e.g. titanium nitride or refractory metal silicide
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N); CHARTERED SEMICONDUCTOR MFG PTE LTD (CHAR-N)
Inventor: SUNDARESAN R
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5721163	A	19980224	US 96661252	A	19960610	199815	B
SG 92608	A1	20021119	SG 972468	A	19970716	200303	N

Priority Applications (No Type Date): US 96661252 A 19960610; SG 972468 A 19970716
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5721163	A		8	H01L-021/8244	
SG 92608	A1			H01L-021/8244	

Abstract (Basic): US 5721163 A

Formation of a SRAM device including a **thin film FET** and a buried contact on a **doped** silicon substrate of first conductivity type, involves (i) forming N+ and P+ source/drain regions of **FET** in the substrate, a gate **oxide layer** over the substrate and a gate electrode over the substrate to form **FET** devices, (ii) deposition of an interconductor device over the **FET** devices, (iii) forming a buried contact via opening through the interconductor **dielectric layer** to the drain region, (iv) depositing a refractory metal silicide gate **electrode layer** to form a buried contact in the opening to the drain region and for forming a gate electrode for another **FET**, (v) forming a mask over the gate layer and patterning the gate layer by etching the gate **electrode layer** to form a gate electrode with exposed surfaces, (vi) forming a **thin film** transistor **gate oxide layer** covering the exposed surfaces of the gate **electrode layer**, (vii) depositing an undoped **semiconductor** polysilicon thin **film** for a **thin film** transistor active channel over the gate **oxide layer**, (viii) performing a Vt **implant** adjustment of the polysilicon **thin film** by **implanting** boron or phosphorus ions in a dose of 1016-1017 atoms/cm3, and (ix) forming a **thin film** transistor source/drain in the polysilicon **thin film**.

ADVANTAGE - The control gate electrode material has a threshold level near the intrinsic level to avoid the problem of TFTs suffering from high negative threshold voltage.

Dwg.2,3E/3

23/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010544909
WPI Acc No: 1996-041862/199605
XRAM Acc No: C96-014197
Formation of metal silicide film on source and drain regions - in mfr. of C-MOSFETs
Patent Assignee: NEC CORP (NIDE)
Inventor: MOGAMI T; TATSUMI T
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 689237	A1	19951227	EP 95109564	A	19950620	199605	B
JP 8070053	A	19960312	JP 9581185	A	19950406	199620	
US 5571735	A	19961105	US 95490653	A	19950616	199650	
EP 689237	B1	19981230	EP 95109564	A	19950620	199905	
DE 69506951	E	19990211	DE 606951	A	19950620	199912	
			EP 95109564	A	19950620		

Priority Applications (No Type Date): JP 9581185 A 19950406; JP 94138827 A 19940621
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 689237	A1	E	19	H01L-021/3205	
Designated States (Regional): DE FR GB					
JP 8070053	A		8	H01L-021/8238	
US 5571735	A		15	H01L-021/265	
EP 689237	B1	E		H01L-021/3205	
Designated States (Regional): DE FR GB					
DE 69506951	E			H01L-021/3205	Based on patent EP 689237

Abstract (Basic): EP 689237 A
A method of mfg. a **semiconductor** device comprises: (a) forming gate **electrodes** via gate **insulating films** on a Si substrate on which an element sepn. region has been formed; (b) forming **insulating films** on at least the side surfaces of the gate electrodes; (c) performing **ion implantation** of **impurities** in the element sepn. region to form source and drain regions of n and p channel type **FETs**; (d) forming metal silicide films on at least source and drain regions by (e) selectively depositing Si **thin films** with **impurity** concentration less than 1019cm-3; (f) amorphising the Si **thin films**, **gate electrodes**, and Si substrate by **ion implantation**; (g) depositing a metal film; (h) heat-treating to form metal silicide; and (i) removing unreacted metal **films** remaining on the **insulating film**.
USE - Method is used in the mfr. of CMOSFETs.
ADVANTAGE - Metal silicide films have the same thickness on both the N and P channel MOSFET regions.
Dwg.6A-D/8
Abstract (Equivalent): US 5571735 A
A method of mfg. a **semiconductor** device comprises the steps of: (a) forming silicon gate **electrodes** on gate **insulating films** on a silicon **semiconductor** substrate on which an

element sepn. region is formed, the silicon gate electrodes having an upper surface and a side surface; (b) forming **insulating films** on the side surface of the silicon gate electrodes; (c) performing **ion implantation** of **impurities** in the element sepn. region to form source and drain regions of N-channel type and P-channel type field effect transistors on the silicon **semiconductor** substrate; (d) selectively depositing silicon films on the source and drain regions and on the upper surface of the silicon gate **electrodes**, the silicon **films** having **impurity** concn. less than 1019 cm-3; (e) amorphising the silicon **films**, the silicon gate **electrodes**, and the silicon **semiconductor** substrate by **ion implantation**; (f) depositing a metal film on the silicon films and on the silicon gate electrodes; (g) performing heat treatment of the metal film to form metal silicide films on the source and drain regions and on the upper surface of the silicon gate electrodes; and (h) removing unreacted metal **films** remaining on the **insulating films**.

6b,6c,6d/8

23/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009049267
WPI Acc No: 1992-176640/199222
XRAM Acc No: C92-080947
XRPX Acc No: N92-133269
Insulated gate **FET** devices and methods - have reduced gate insulation stress
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: REYNOLDS J; SMAYLING M C
Number of Countries: 008 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 487022	A2	19920527	EP 91119712	A	19911119	199222	B
EP 487022	A3	19920715	EP 91119712	A	19911119	199334	
US 5275961	A	19940104	US 90618351	A	19901123	199402	
			US 92915036	A	19920716		
JP 6104442	A	19940415	JP 91307684	A	19911122	199420	
US 5407844	A	19950418	US 90618351	A	19901123	199521	
			US 92915036	A	19920716		
			US 93102682	A	19930805		
			US 94228164	A	19940415		
EP 487022	B1	19970423	EP 91119712	A	19911119	199721	
DE 69125794	E	19970528	DE 625794	A	19911119	199727	
			EP 91119712	A	19911119		
KR 212408	B1	19990802	KR 9120875	A	19911122	200104	

Priority Applications (No Type Date): US 90618351 A 19901123; US 92915036 A 19920716; US 93102682 A 19930805; US 94228164 A 19940415
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 487022	A2	E	83	H01L-029/784	
Designated States (Regional): DE FR GB IT NL					
EP 487022	A3			H01L-029/784	
US 5275961	A		9	H01L-021/00	Cont of application US 90618351
JP 6104442	A		65	H01L-029/784	
US 5407844	A		70	H01L-021/265	Cont of application US 90618351 Div ex application US 92915036 Cont of application US 93102682 Div ex patent US 5275961
EP 487022	B1	E	75	H01L-029/772	
Designated States (Regional): DE FR GB IT NL					
DE 69125794	E			H01L-029/772	Based on patent EP 487022
KR 212408	B1			H01L-027/00	

Abstract (Basic): EP 487022 A

IGFET comprises: **thin gate insulator layer** formed on a **semiconductor** layer of first type; control gate (458) having first and second lateral margins; source and drain regions (464, 466) of second type formed respectively adjacent the second and first lateral regions; and a channel between source and drain.

Pref. a first portion (462) of the control gate adjacent the first lateral margin is formed of dielectric and a second portion (460) adjacent the second lateral margin is formed of conductive material.

USE/ADVANTAGE - In stressful electrical or electronic

environments, esp. automobile electrical systems. Transistor has reduced gate insulator stress. (claimed)

Dwg.14g/29

Abstract (Equivalent): EP 487022 B

A method of simultaneously fabricating an insulated-gate-field-effect transistor having reduced gate insulator stress and a bipolar transistor, the method comprising the steps of: providing a **semiconductor** substrate (150) of a first conductivity type, the substrate having a face; providing a first epitaxial layer (156) of the first conductivity type on the face of the substrate, the first epitaxial layer has a face and is divided into a first region and a second region; forming a first region (410,774) of a second conductivity type opposite the first conductivity type in the face of the first region of the first epitaxial layer; forming a second tank region (456) of the first conductivity type in the face of the second region of the first epitaxial layer; forming a tank region (454) of the second conductivity type in the second tank region in the face of the first epitaxial layer; forming a fourth tank region (412,778) of the first conductivity type in the first tank region in the face of the first epitaxial layer; forming a gate structure (458) insulation disposed over the face of the second region of the first epitaxial layer; the gate structure is comprised of a conductive portion (45) and a nonconductive portion (462) which is situated over the third tank region; simultaneously forming regions of a second conductivity type, the regions comprising: a) a source region (464) at the face of the first epitaxial layer in the second tank region and spaced from the third tank region, b) a drain regions (466) at the face of the first epitaxial layer in the tank region and spaced from the nonconductive portion of the gate structure, c) a collector region (414,784) at the face of the first epitaxial layer in the first tank region and spaced from the fourth tank region, and d) an emitter region (416,786) at the face of the first epitaxial layer in the fourth tank region; and forming a base region (422,788) at the face of the first epitaxial layer in the fourth tank region and spaced from the emitter region.

Dwg.1/29

Abstract (Equivalent): US 5407844 A

The IGFET is mfd. by (a) providing a 1st **conductivity** type 1st epitaxial **layer** on a 1st tape substrate having 1st and 2ns regions, (b) forming 1st and 2nd tank regions of 2nd-or 1st-type conductivity in the 1st and 2nd regions respectively, (c) forming 3rd and 4th tank regions of 2nd-an 1st-type conductivity in the 2nd and 1st tank regions respectively, (d) forming a gate gate structure over the 2nd region, composed of conductive and non-conductive portions (e) simultaneously forming 2nd-type regions and (4) forming a base region at the 1st epitaxial layer in the 4th tank region and spaced from the emitter region.

ADVANTAGE - Reduced gate insulator stress (claimed. Resistant to high voltage transients such as encountered in automotive electrical systems.

Dwg.12/29

US 5275961 A

Insulated gate field effect transistor is fabricated by a method in which a first tank region (454) e.g. n-tank is **implanted**, followed by a high-voltage p-tank (456), localised oxide (210) defining a moat for the first region. A control gate (458) is formed such that a lateral margin of the second tank region is beneath a portion of the control gate. Source and drain regions (464, 466) are **implanted**. The gate is **doped**, e.g. with P, while a section (462) is covered

with a mask, so that the section does not receive **dopant** and remains non-conductive.

ADVANTAGE - Gate oxide breakdown due to high electric fields is prevented.

Dwg. 14g/2

9

23/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008998002
WPI Acc No: 1992-125275/199216
XRAM Acc No: C92-058431
XRPX Acc No: N92-093681
SOI type field effect transistor - having improved characteristic due to prevention of over-etching of source-drain region
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: AJIKA N; YAMAGCHI Y; YAMANO T; YAMAGUCHI Y
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 480635	A	19920415	EP 91309095	A	19911003	199216	B
JP 4147629	A	19920521	JP 90271727	A	19901009	199227	
US 5341028	A	19940823	US 91770041	A	19911003	199433	
EP 480635	B1	19950809	EP 91309095	A	19911003	199536	
US 5444282	A	19950822	US 91770041	A	19911003	199539	
			US 94268877	A	19940630		
DE 69111963	E	19950914	DE 611963	A	19911003	199542	
			EP 91309095	A	19911003		

Priority Applications (No Type Date): JP 90271727 A 19901009
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 480635	A	E	21		
Designated States (Regional): DE FR GB					
JP 4147629	A		12	H01L-021/336	
US 5341028	A		18	H01L-027/01	
EP 480635	B1	E	23	H01L-029/786	
Designated States (Regional): DE FR GB					
US 5444282	A		18	H01L-027/01	Cont of application US 91770041 Cont of patent US 5341028
DE 69111963	E			H01L-029/786	Based on patent EP 480635

Abstract (Basic): EP 480635 A

A **semiconductor** device comprising a field effect transistor (**FET**) and having a SOI structure, consists of (a) a **semiconductor** layer (13) formed on an **insulator layer** (12); (b) a channel region of first conductivity type (14) formed in the **semiconductor** layer; (c) additional source/drain regions (15,16) of second conductivity type formed in **semiconductor** layer (13) adjacent to left and right sides of channel region; (d) a gate electrode (20) formed above the channel region (14) with a **thin, dielectric film** (19) therebetween; (e) a first sidewall spacer (25) on left and right sidewalls of gate electrode (20); (f) a metal layer (27) having resistance to etching, formed at surface of **semiconductor** layer (13) outside region subtended by first sidewall spacers (25); (g) a second sidewall spacer (26) covering the outer surface of the first sidewall spacer (25); and (h) source/drain regions (17,18) having **impurity** concn. higher than that of additional source/drain (15,16) and formed in **semiconductor** layer (13) outside region subtended by second sidewall spacers (26).

USE/ADVANTAGE - Provides a device of the SOI-MOSFET type, having

improved transistor characteristic by suppressing decrease of film thickness in the **semiconductor** layer caused by over-etching. The structure is free of soft error and latch-up phenomenon. As a result of maintaining low resistance of the source and drain regions, the VD-ID characteristic is improved.

Abstract (Equivalent): EP 480635 B

A method of manufacturing a **semiconductor**-on-insulator device comprising the steps of: (a) forming a **semiconductor** layer (13) of a first conductivity-type on an **insulator layer** (12); (b) forming a **dielectric thin film** (19) on the **semiconductor** layer (13); (c) forming a gate electrode (20;120) on the **dielectric thin film** (19); (d) forming lightly **doped** source/drain regions (15,16) by **implanting dopant impurities** of a second conductivity-type into the **semiconductor** layer (13) using the gate electrode (12) as a mask, and (e) forming source/drain regions (17;18) adjacent to the lightly **doped** source/drain regions (15,16), the source/drain regions (17,18) having a **dopant impurity** concentration higher than that of the lightly **doped** source/drain regions (15,16), by **implanting dopant impurities** of the second conductivity-type into the **semiconductor** layer (13) using the gate **electrode** (20) and sidewall **spacers** each side of the gate electrode (20) as a mask; which method is characterised by the following steps which are performed following step (d) and preceding step (e); (f) depositing, by chemical vapour deposition, a **thin film** of **insulator** material on the exposed surfaces of the gate electrode (20) and the **dielectric thin film** (19); (g) etching the **thin** film of **insulator** material and **dielectric thin film** to expose the surface of the gate electrode (12) and the surface of the **semiconductor** layer (13) and to delineate a first sidewall spacer (25) of the sidewall spacers adjacent to each side of the gate electrode (12); (h) forming a metallic **layer** on the gate **electrode** (12) and surface of the **semiconductor** layer (13) to the exclusion of the surface of each first sidewall spacer; (i) depositing, by chemical vapour deposition, a **film** of **insulator** material on the exposed surfaces of the metallic layer and each first sidewall spacer and (j) etching the **film** of **insulator** material, using an etchant against which the metallic layer is resistant, to delineate a second sidewall spacer of the sidewall spacers adjacent to each first sidewall spacer.

(Dwg.2/9

Abstract (Equivalent): US 5444282 A

Semiconductor device comprises a **semiconductor layer** over an **insulator layer**; a channel region of a 1st **conductivity** in **semiconductor layer**; 1st source and drain regions of 2nd conductivity adjacent channel region; a gate electrode above channel region with a dielectric in between; 1st sidewall spacers on left and right sidewalls of gate electrode; an etch-resistant metal layer outside area where sidewall spacers are formed; 2nd sidewall spacers outside 1st; 2nd source and drain regions of high concn. than 1st outside 2nd sidewall spacers; and interconnection layer connected to metal layer. The metal layer is of cobalt silicide.

USE/ADVANTAGE - Used as MOSFETs. Device has improve transistor characteristics by suppressing decrease of **semiconductor** film thickness due to over-etching.

Dwg.5/9

US 5341028 A

Semiconductor device includes a thin **film** SOI-MOSFET with **insulator layer** (12) on a Si substrate (11), over which a **thin** Si **layer** (13) has a channel region (14) of low p-type **impurity** concn. (14). Additional source (15) and drain (16) regions are formed adjacent to the channel region above which is a **gate** region (14). A **thin** sidewall **spacer** (25) is formed at the gate electrode sidewall (20) and a metal layer (27) is formed on the Si layer not covered with gate **electrode** or sidewall **spacer**, and on the gate **electrode**. A second sidewall **spacer** (26) is formed at the outer surface of the first spacer.

ADVANTAGE - Improved transistor characteristics by suppression of over-etching in the **semiconductor** layer.

Dwg.5/9

23/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008720574
WPI Acc No: 1991-224591/199131
XRAM Acc No: C91-097533
XRPX Acc No: N91-171434
Formation of **FET** with LDD structure - comprises **implanting** **impurities** through non-etched uniform films and thus providing stable **impurity** profiles
Patent Assignee: NEC CORP (NIDE)
Inventor: ITOH H
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 439173	A	19910731	EP 91100911	A	19910124	199131	B
JP 3220729	A	19910927	JP 9016839	A	19900125	199145	
US 5120673	A	19920609	US 91645770	A	19910125	199226	
EP 439173	B1	19950419	EP 91100911	A	19910124	199520	
DE 69108938	E	19950524	DE 608938	A	19910124	199526	
			EP 91100911	A	19910124		

Priority Applications (No Type Date): JP 9016839 A 19900125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 439173	A				
Designated States (Regional): DE FR GB					
US 5120673	A		12	H01L-021/265	
EP 439173	B1	E	13	H01L-029/772	
Designated States (Regional): DE FR GB					
DE 69108938	E			H01L-029/772	Based on patent EP 439173

Abstract (Basic): EP 439173 A

Lightly **doped** and heavily **doped** regions are formed by **implanting** through a gate oxide or a **gate** oxide and **thin** poly which are unetched. A gate oxide (22) is formed on a substrate (21) of a first conductivity type and gate electrode (25) is formed on a predetermined portion of the gate oxide. The gate electrode (25) is then used as a mask to **implant** an **impurity** of a second conductivity type, through the gate oxide (22) thus forming the lightly **doped** regions (21a). A **doped** poly **film** (26), a protective **oxide** (27) and an undoped poly (28) are then formed sequentially over the entire surface. The undoped poly (28) is then anisotropically etched, to form a side wall (28a) on a portion of the protective oxide (27) covering a side surface of the gate electrode (25) and the protective oxide (27) is exposed. Exposed portions of the protective oxide (27) are removed. The gate electrode and side walls are then used as a mask to **implant** an **impurity** of a second conductivity, thus forming heavily **doped** regions (21b). The side walls are then removed.

ADVANTAGE - **Impurities** are **implanted** through films of a uniform thickness and so the **impurity** profiles are stable. Device characteristics stay within the design specification and therefore the production yields of the **FET** is improved. (9pp Dwg.No.2F/4)

Abstract (Equivalent): EP 439173 B

A process of fabricating a field effect transistor comprising the steps of: a) preparing a **semiconductor** substrate of a first conductivity type having a major surface; b) forming a gate **oxide film** on said major surface; c) forming a gate electrode on a predetermined portion of said gate **oxide film**; and d) forming lightly **doped impurity** regions and heavily **doped impurity** regions wherein said step d) comprises the substeps of: d-1) carrying out a first **ion-implantation** through said gate **oxide film** for **doping** said **semiconductor** substrate with **impurity** atoms of a second conductivity type opposite to said first conductivity type, thereby forming said lightly **doped impurity** regions, said gate electrode serving as a mask during said first **ion-implantation**; d-2) covering the entire surface of the structure with a **doped** polysilicon film overlain by a protective **oxide film**; d-3) covering said protective **oxide film** with an intentionally undoped polysilicon film; d-4) anisotropically etching said intentionally undoped polysilicon film thereby forming a side wall on a portion of said protective **oxide film** covering a side surface of said gate electrode covered with said **doped** polysilicon **film**, said protective **oxide film** being exposed on both sides of said side wall; d-5) removing exposed portions of said protective **oxide film** and of said **doped** polysilicon film; d-6) carrying out a second **ion-implantation** using said gate electrode covered with said **doped** polysilicon film and said side wall as a mask for **doping** said **semiconductor** substrate with **impurity** atoms of said second conductivity type, thereby forming said heavily **doped impurity** regions; and d-7) removing said side wall.

(Dwg.0/4

Abstract (Equivalent): US 5120673 A

Field, effect transistor is made by firstly preparing a **semiconductor** substrate of a first conductivity type having a major surface. A gate **oxide film** (I) is then formed on the major surface. A gate electrode (II) is formed on a predetermined portion of film (I). A first **ion-implantation** is **conducted** through **film** (I) for **doping** the substrate with **impurity** atoms of a second conductivity type, opposite to the first conductivity type, thereby forming **doped impurity** regions, electrode (II) serving as a mask during the first **ion-implantation**. The entire surface of the structure is covered with **doped** polysilicon film, overlaid by a protective **oxide film** (III).

Film (III) is covered with an intentionally undoped polysilicon film (IV). Film (IV) is anisotropically etched for forming a side wall on a portion of film (III), covering a side surface of **electrode** (II), a **film** (III) being exposed on both sides of the side wall. Exposed portions of film (III) are removed, without etching the **doped** polysilicon.

A second **ion-implantation** is conducted through the **doped** polysilicon, using electrode (II) and the side wall as a mask for **doping** the substrate with **impurity** atoms of the second conductivity type, thereby forming heavily **doped impurity** regions. Finally, the side wall is removed.

ADVANTAGE - Field effect transistor is made with the LDD structure having a stable **impurity** profile.

Dwg.4F/4

23/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008442893
WPI Acc No: 1990-329893/199044
XRAM Acc No: C90-143157
XRPX Acc No: N90-252553
Prodn. of a refractory metal self-aligned gate - using a refractory metal sidewall structure formed on an **insulation layer** as gate and **implantation** mask
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: KOHNO Y; OKU T
Number of Countries: 004 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2230899	A	19901031	GB 907215	A	19900330	199044	B
JP 2271538	A	19901106	JP 8993579	A	19890412	199050	
FR 2649535	A	19910111	FR 904662	A	19900411	199109	
US 5187112	A	19930216	US 90504837	A	19900405	199309	
GB 2230899	B	19930519	GB 907215	A	19900330	199320	
US 5250453	A	19931005	US 90504837	A	19900405	199341	
			US 92953049	A	19920929		

Priority Applications (No Type Date): JP 8993579 A 19890412
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5187112	A		11	H01L-021/265	
US 5250453	A		11	H01L-021/265	Div ex application US 90504837 Div ex patent US 5187112
GB 2230899	B			H01L-029/64	

Abstract (Basic): GB 2230899 A

Semiconductor device is mfd. by: plating an **insulating film** (3) onto active layer (2) on a substrate (1); plating a refractory metal layer (4') onto the sidewall of the **insulating film** to form a gate electrode; **implanting** a high concn. **layer** (5) using the **insulating film** and refractory metal as mask; removing the **insulating film** and **implanting** an intermediate concn. **doping** layer (8) using the refractory metal as mask; and forming a source electrode (6) on the high concn. **layer** and a drain **electrode** (7) on the intermediate concn. layer.

The sidewall thickness is tailored to equal the desired **gate length**; the sidewall is formed by anisotropic etching, pref. by RIE using CFH3 and O2. The **doping** concn. of the high concn. layer is 3 x 10 power(13) per sq. cm. and of the intermediate concn. layer is 7 x 10 power(12) per sq. cm. The refractory metal is WSix, WN or WSiN.

USE/ADVANTAGE - In prodn. of fine pattern gate and an offset gate of a refractory metal self-aligned gate GaAs **FET**. Fine pattern metal gate is formed without photolithography, and gate-drain breakdown voltage is enhanced while source resistance is kept low. (34pp Dwg.No.1e-g/5)

Abstract (Equivalent): GB 2230899 B

A production method of a **semiconductor** device, comprising: a first process of plating an **insulating film** on an active

layer produced on a **semiconductor** substrate and processing said **insulating film**; a second process of plating refractory metal on the entire surface of said **semiconductor** substrate and applying a processing to said refractory metal so as to remain a portion thereof at the side wall of said **insulating film**, thereby to produce a gate electrode; a third process of producing a gate electrode; a third process of producing a high concentration **doping layer** by **conducting ion implantation** by using said **insulating film** and refractory metal as a mask; a fourth process of removing said **insulating film** and producing an intermediate concentration **doping** layer by **ion implantation** by using said refractory metal as a mask; and a fifth process of producing a source electrode on said high concentration **doping** layer and producing a drain electrode on said intermediate concentration **doping** layer.

Dwg.1/1

Abstract (Equivalent): US 5250453 A

Method comprises (a) forming an active region in and at a surface of a **semiconductor** substrate, (b) depositing a 1st **insulating film** on the active region, (c) removing a portion of the 1st **insulating film** at the active region, leaving a sidewall of the 1st **insulating film** perpendicular to the substrate surface, (d) depositing a refractory metal material **layer** on the 1st **insulating film** and surface of the substrate, (e) removing the refractory material except for a residual portion at the sidewall of the 1st **insulating film** to produce a gate electrode, (f) producing an intermediate **dopant** concn. region in the substrate by **ion implantation** using the 1st **insulating film** and gate **electrode** as a mask, (g) depositing a 2nd insulating **film** on the 1st insulating **film**, gate **electrode** and substrate surface, (h) removing the 2nd **insulating film** except for a residual portion at the gate electrode, (i) removing the 1st **insulating film**, (j) producing relatively high **dopant** concn. regions in the **semiconductor** substrate by **ion-implantation** using the gate electrode and the residual portion of the 2nd **insulating film** as mask, and (k) producing a drain electrode on the relatively high **dopant** concn. regions at a 1st side of the gate electrode where the intermediate **dopant** concn. region is disposed and producing a source electrode on the other of the relatively high **dopant** regions opposite the 1st side of the gate electrode.

USE/ADVANTAGE - Used for producing a **narrow gate** and an offset gate of a refractory metal in a self-aligned gate GaAs **FET**, without using photolithography, increased gate-drain breakdown voltage, and low source resistance.

Dwg.2e/5

US 5187112 A

Method of forming a **semiconductor** device using a **semiconductor** substrate on which is applied an active region and a first **insulating film**. The **insulating film** is removed from the active region before depositing a refractory metal layer over the whole surface. Part of the refractory metal layer is then removed to form a gate **electrode**. The **insulating film** is removed and intermediate concn. regions formed by **ion implantation** using the gate electrode as a mask. A second **insulating film** is formed on the gate electrode. High **dopant** concn. regions are then formed by **ion implantation** using the gate **electrode** and second

insulating film as a mask. Finally a drain electrode is formed on the first high **dopant** level region and a source electrode is formed on the second side of the gate electrode. ADVANTAGE - Device is produced without the need for photolithography.
(Dwg.3b/5

23/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008278490
WPI Acc No: 1990-165491/199022
XRAM Acc No: C90-072155
XRPX Acc No: N90-128466
Silicon-on-**insulator** metal **oxide semiconductor** with **thin film FET** - body region for improved withstand voltage between source and drain
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: NISHIMURA T; YAMAGUCHI Y
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 370809	A	19900530	EP 89312166	A	19891123	199022	B
JP 2144969	A	19900604	JP 88299136	A	19881125	199028	
US 5125007	A	19920623	US 89439680	A	19891122	199228	
EP 370809	B1	19940302	EP 89312166	A	19891123	199409	
DE 68913444	E	19940407	DE 613444	A	19891123	199415	
			EP 89312166	A	19891123		
US 5343051	A	19940830	US 89439680	A	19891122	199434	
			US 91753285	A	19910830		
			US 9358814	A	19930510		
US 5424225	A	19950613	US 89439680	A	19891122	199529	
			US 91753285	A	19910830		
			US 9358814	A	19930510		
			US 94269287	A	19940630		

Priority Applications (No Type Date): JP 88299136 A 19881125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 370809	A				
Designated States (Regional): DE FR GB					
US 5125007	A		25	H01L-027/01	
EP 370809	B1	E	28	H01L-029/784	
Designated States (Regional): DE FR GB					
DE 68913444	E			H01L-029/784	Based on patent EP 370809
US 5343051	A		25	H01L-029/04	Cont of application US 89439680 Cont of application US 91753285 Cont of patent US 5125007
US 5424225	A		26	H01L-021/265	Cont of application US 89439680 Cont of application US 91753285 Div ex application US 9358814 Cont of patent US 5125007 Div ex patent US 5343051

Abstract (Basic): EP 370809 A

MOSFET comprises: an insulator substrate having a **semiconductor** layer formed on it; a channel region of a first conductivity type formed in **semiconductor** layer; a source region of second **conductivity** formed in **semiconductor layer** contacting side of channel region, and a drain region of second conductivity formed contacting other side of channel region; a body region of first conductivity type having a higher **impurity** concn. than channel region and formed in contact with at least a part of

channel part of channel region and at least a part of a periphery of source region; a **gate dielectric thin film** formed on channel region; a gate **electrode** formed on **dielectric film**; a first **conductor** connected in common to source and body-regions; a second conductor connected to gate electrode; a third conductor connected to drain region. Pref. the body region surrounds channel, source and drain regions.

USE/ADVANTAGE - Simplified mfr. of SOI-MOSFET comprising a body region in which a planar area occupied by SOI-MOSFET is not increased. (28pp Dwg.No.1/24

Abstract (Equivalent): EP 370809 B

A MOS field effect transistor comprising: an insular substrate (2); a **semiconductor** layer (3) formed on said insulator substrate (2); a channel region (6) of a first conductivity type formed in said **semiconductor** layer (3); a source region (8) of a second conductivity type formed in said **semiconductor** layer (3) being in contact with one end of said channel region (6); a drain region (9) of the second conductivity type formed in said **semiconductor** layer (3) being in contact with the other end of said channel region (6); a body region (7) of the first conductivity type having a higher **impurity** concentration than that of said channel region (6) and being formed in contact with at least a part of a periphery of said source region (8) in said **semiconductor layer** (3); a **gate electrode thin film** (4) formed on said channel region (6); a gate electrode (5) formed on said **dielectric** thin **film** (4); a first **conductor** (14a) connected in common to said source region (8) and said body region (7); a second conductor (14b) connected to said gate electrode (5); and a third conductor (14c) connected to said drain region (9); which MOS field effect transistor is characterised in that: said body region (7) surrounds said channel region (6), said source region (8) and said drain region (9).

(Dwg.1/24

Abstract (Equivalent): US 5424225 A

A MOSFET is mfd. by (a) forming a 1st **conductivity** type Si **layer** (3) on an **insulating** substrate (2), (b) covering the Si layer (3) with a nitride layer (16), (c) covering part of the nitride layer with a 1st resist (17), (d) etching the nitride layer using the resist as mask, (e) forming a body region (7) in an outer periphery of the transistor region of the Si layer by **implanting** 1st type ions (18) using the resist as mask, (f) forming an isolation **oxide film** (10) and diffusing the **impurity** toward the centre of the transition by thermally oxidising the Si layer using the nitride layer as mask after removing the resist, leaving the body region at least under a birds beak of the isolation **oxide film** in a periphery of the transistor region, (g) forming a gate **insulating film** (4) and a gate electrode (5) using a 2nd resist (20) after removing the nitride film, (h) forming source (8) and drain (9) regions by **implanting** 2nd-type ions (19) using the 2nd resist and isolation **oxide film** as masks, (i) covering the Si and gate **electrode layers** with an **interlayer insulating film** (11) after removing the 2nd resist, (j) forming a contact hole (12a) exposing not only a part of the source but also a part of the body region, and (k) forming a conductor (14a) to be connected to the source region and body region through the contact hole.

USE/ADVANTAGE - As an 501-MOSFET. Relatively simple mfr. Dwg.5d/24

US 5343051 A

An MOS **FET** has a **semiconductor** layer (3) formed on an **insulation layer** (2), a second **conductivity** type source region (8) contacting the **insulation layer** surface and one side of a first type channel region (6), and a second type drain region (9) contacting the **insulation layer** and other side of the channel. A gate electrode (5) is formed on a **gate dielectric thin film** formed on the channel.

A body region (7) of first type has higher **impurity** concn. than the channel and contacts the **insulation layer** and part or all of the channel, while making lateral contact only with the source and/or drain in the **semiconductor** layer. The body region extends along a boundary between channel and source.

ADVANTAGE - Provides a body region without increasing the planar area of the MOSFET and without complicating the mfg. process.

Dwg.2/24

US 5125007 A

MOS field effect transistor comprises: (a) an insulator substrate; (b) a **semiconductor** layer formed on (a); (c) a channel region of a first **conductivity** type formed in **layer** (b); (d) a source region of a second **conductivity** type formed in **layer** (b), in contact with one side of region (c); (e) a drain region of the second **conductivity** type, formed in **layer** (b), in contact with the other side of region (c); (f) a body region of the first conductivity type having a higher **impurity** concn. than that of region (c) and being formed in lateral contact with at least a part of region (c), and at least a part of a periphery of region (d) in layer (b); (g) a gate dielectric of region (d) in layer (b); (g) a **gate dielectric thin film** formed on region (c); (h) a gate **electrode** formed on **film** (g); (i) a first conductor connected to electrode (h); and (k) a third conductor connected to region (e). Region (f) surrounds regions (c), (d) and (e) and further extends along a boundary between regions (c) and (d) in a lower partial layer. ADVANTAGE - A SOI-MOSFET is provided comprising a body region in which a planar area occupied by SOI-MOSFET is not increased.

(Dwg.1/24

23/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007921924
WPI Acc No: 1989-187036/198926
XRAM Acc No: C89-082670
XRPX Acc No: N89-142831
Schottky gate field effect transistor - with gate electrode self aligned with source and drain high **impurity** concn. regions
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: ITO K
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2211350	A	19890628	GB 8823975	A	19881013	198926	B
JP 1109771	A	19890426				198926	
FR 2622355	A	19890428				198928	
US 4843024	A	19890627	US 88258498	A	19881017	198933	
GB 2211350	B	19920212				199207	

Priority Applications (No Type Date): JP 87268439 A 19871022
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2211350	A		16		
US 4843024	A		8		

Abstract (Basic): GB 2211350 A

A Schottky gate field effect transistor pref GaAs MESFET, is produced by: producing a first **thin film** pattern pref. SiO2, at a gate electrode production region on a first **conductivity** type **semiconductor layer** which is produced in a surface regin of a **semiconductor** substrate substrate; producing first conductivity type high concentration regions in substrate by **impurity ion implantation**; producing a second **thin film** pref. SiN, on substrate and of same thickness as first **thin film**; applying photoresist on second **thin film** to form a flat surface, which has same etching speed as second **thin film**; etching photoresist until top portion of first **thin film** is exposed; removing first **thin film** pattern by etching; producing photoresist patterns on both sides of second **thin films** so as to have a larger aperture than that of second **thin films**; producing a **gate electrode** which has portions on both of second **thin films** by vapour deposition and lift off utilising photo resist patterns.

USE/ADVANTAGE - Production of Schottky gate **FET**'s with gate electrode self aligned with source/drain high **impurity** concentration regions at high controllability. Gate resistance can be suppressed even with a short **gate length**.

11/2

Abstract (Equivalent): GB 2211350 B

A method of producing a Schottky gate field effect transistor comprising the steps of: producing a first **thin film** pattern at a gate electrode production region on a first **conductivity** type **semiconductor layer** which is produced in a surface region of a **semiconductor** substrate;

producing a second **thin film** on said **semiconductor** substrate having said first **thin film** pattern, to the same thickness as said first **thin film**; applying a photoresist on said second **thin film** such that the surface thereof becomes flat, which has the same etching speed as said second **thin film**; etching said photoresist and the portion of the second thin **film** over the first **thin film** until the top portion of said first **thin film** pattern is exposed; removing said first thin filmpattern by etching to leave an aperture in the second **thin film**; producing a photoresist pattern on said second **thin film** so as to have a larger aperture than that of said second **thin film**; and producing a gate electrode which has a portion on said second **thin film** by vapor deposition and lift off utilizing said photoresist pattern.

Abstract (Equivalent): US 4843024 A

A Schottky gate field effect transistor is produced by firstly depositing a first **thin film** on a first **conductivity** type **semiconductor layer** which is disposed in and at a surface of a **semiconductor** substrate (I). First conductivity type high **impurity** concn. regions are produced in (I), adjacent the first **thin film**, by **impurity ion implantation**. A second **thin film** is deposited on the surface of (I), and on the first **thin film**, of the same thickness as the first **thin film**. A first mask is applied on the second **thin film**, in sufficient thickness that its exposed surface becomes flat.

The first mask and the second film are etched until the first **thin film** is exposed. The first **thin film** is removed, leaving the second **thin film** as two regions with an aperture between them. Part of the second **thin film** regions are masked, leaving an unmasked portion between them overlying the larger than the aperture. Finally, a gate electrode metal is deposited forming a Schottky barrier with the layer in the aperture and on the unmasked portions of the second **thin film** regions.

ADVANTAGE - Method is provided for producing a self-aligned Schottky gate field effect transistor, with high deg. of process controllability. (8pp)

23/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004328867
WPI Acc No: 1985-155745/198526
XRAM Acc No: C88-142552
XRPX Acc No: N88-245053
Gallium arsenide MESFET with low source resistance - has satisfactory leakage current, produced by **ion implantation** for use in microwave band
Patent Assignee: MATSUSHITA ELECTRIC WORKS LTD (MATW); MATSUSHITA ELECTRONICS CORP (MATE)
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 60086866	A	19850516	JP 83194090	A	19831019	198526	B
US 4782031	A	19881101	US 8722597	A	19870304	198846	

Priority Applications (No Type Date): JP 83194090 A 19831019
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 60086866	A		9		

Abstract (Basic): JP 60086866 A

A **FET** mfd. by: forming a gate electrode pref. TiN or WSi, on a surface of a first **semiconductor** region located on a semi-insulating surface pref. GaAS; forming a **thin film** pref. SiO2 or SiN by plasma CVD, on a first **semiconductor** region and on top and side surface of gate electrode; selectively surface of first **semiconductor** region by selectively removing **thin film** disposed away from side surfaces of gate electrode at a fixed distance; **ion implanting** an **impurity** of one conductivity type through exposed surface of first **semiconductor** region and through unremoved **thin film**, forming: (a) a pair of second **semiconductor** regions of one conductivity type deeper than first **semiconductor** region at a portion beneath exposed surface of first **semiconductor** region; (b) a pair of third **semiconductor** regions of one conductivity type thinner than first **semiconductor** srface occupied by **gate electrode** and **thin film** formed on side surface of gate electrode; forming a source electrode and drain electrode on surface of second **semiconductor** regions, respectively respectively.

Pref. the **impurity** concn. of second and third **semiconductor** regions is higher than first **semiconductor** region, and first **semiconductor** is formed by epitaxial growth or **ion implanting**.

USE/ADVANTAGE - **FET** with low source/drain leakage current and low source resistance part. for use in a microwave band. (First major country equivalent to J60086866-A)

2/4

Abstract (Equivalent): US 4782031 A

A **FET** mfd. by: forming a gate electrode pref. TiN or WSi, on a surface of a first **semiconductor** region located on a semi-insulating surface pref. GaAS; forming a **thin film** pref. SiO2 or SiN by plasma CVD, on a first **semiconductor** region and on top and side surface of gate electrode; selectively surface of

first **semiconductor** region by selectively removing **thin film** disposed away from side surfaces of gate electrode at a fixed distance; **ion implanting** an **impurity** of one conductivity type through exposed surface of first **semiconductor** region and through unremoved **thin film**, forming: (a) a pair of second **semiconductor** regions of one conductivity type deeper than first **semiconductor** region at a portion beneath exposed surface of first **semiconductor** region; (b) a pair of third **semiconductor** regions of one conductivity type thinner than first **semiconductor** srface occupied by **gate electrode** and **thin film** formed on side surface of gate electrode; forming a source electrode and drain electrode on surface of second **semiconductor** regions, respectively respectively.

Pref. the **impurity** concn. of second and third **semiconductor** regions is higher than first **semiconductor** region, and first **semiconductor** is formed by epitaxial growth or **ion implanting**.

USE/ADVANTAGE - **FET** with low source/drain leakage current and low source resistance part. for use in a microwave band. (First major country equivalent to J60086866-A) (9pp Dwg.No.2/4)

23/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003318711
WPI Acc No: 1982-G6720E/198223
High sensitivity v-form **FET** - has blocking **conductive layer** separation of gate from source and drain in V
Patent Assignee: BENEKING H (BENE-I); LICENTIA PATENT-VERW GMBH (LICN)
Inventor: BENEKING H
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3040873	A	19820603	DE 3040873	A	19801030	198223	B
DE 3040873	C	19840223				198409	
US 4466008	A	19840814	US 81312811	A	19811019	198435	

Priority Applications (No Type Date): DE 3040873 A 19801030
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3040873	A		11		

Abstract (Basic): DE 3040873 A
The simplified construction is for a vertical, ie 'V', formation high sensitivity **FET**. The source (4) and drain (2) are separated from one another by an **insulating layer** (3) and at the end faces in the 'V' formation the source and drain are able to conduct to the **gate** (7) through a **thin** diffused or **ion implanted conducting layer** (6).

The **insulating layer** (3) is broken by the 'V' formation (5) going through it deep enough to reach into the drain (2) zone. The **thin** epitaxial **conducting layer** (6) lines the inner face of the 'V' and is in contact on its upper side with the Schottky gate (7). The source (4) forms an upper face at the top of the 'V' (5) with an electrode (S,10) connection. In order to form the self blocking layer (6) between gate (7) source (4) and drain (2) the **conducting layer** (6) is 0.1 micrometer thick and has a concentration of 10 to power 16 atoms per cc, or is 0.2 micrometer thick with a **doping** concentration of 10 to power 17 atoms cc.

Abstract (Equivalent): US 4466008 A
The field effect transistor comprises a **semiconductor** body, a source region and a drain region arranged vertically in the **semiconductor** body. An **insulating layer** separates the source region from the drain region. A rectifying metal/**semiconductor** contact forms a gate electrode and arranged on a side surface of the **semiconductor** body and a **thin conductive layer** at the side surface and bridges the **insulating layer** at least in the region beneath the gate electrode.

Pref. the rectifying metal/**semiconductor** is applied to the channel in a depression in the **semiconductor** body. The **thin conductive layer**, which is pref. a **semiconductor** layer, forms the controllable channel and may be produced epitaxially, by diffusion or by **ion implantation**.

USE - By selecting the **doping** and thickness of this layer, field effect transistors may be produced which are either conductive or self-blocking when there is no gate voltage. (5pp)

23/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003178701
WPI Acc No: 1981-39252D/198122
Mosfet with precisely formed diffusion regions - is made using laser beam to diffuse **impurities**
Patent Assignee: NIPPON ELECTRIC CO (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 56038868	A	19810414				198122	B

Priority Applications (No Type Date): JP 79114593 A 19790906

Abstract (Basic): JP 56038868 A

FET is made by forming a **gate thin oxide** (SiO2) **layer** (13) and a field thick **oxide** (SiO2) **layer** (12) on a **semiconductor** substrate (11) of p-type Si, then forming a photo resist **layer** (14) on the **oxide layers**, and exposing and developing the resist layer to form openings (15a, 15b) to expose the gate **oxide layer** (13) partially. n-type **ion impurities** are **implanted** followed by etching off the exposed parts of the gate **oxide layer** (13) to form openings (17a,17b), and removing the photo resist layer.

The substrate is heated in N2 to diffuse the **impurities** to form n-type diffusion regions (16a, 16b) in the substrate, followed by depositing aluminium on the substrate selectively to form a gate electrode (18) on the gate **oxide layer** (13) and wiring layers (19a, 19b) connected electrically to the regions with ohmic contact. Second n-type **impurities** are **implanted** into the substrate through the gate **oxide layer**.

Laser beam is directed at the **implanted** second **ion impurities** to diffuse the second **impurities** to form a source region (20a) and a drain region (20b). The wiring **layers** and the gate **electrode** are covered with an **insulating layer** (20) and another wiring layers (21a,21b) formed on the **insulating layer** (20).

The second **impurities** are diffused by the layer, so that the diffusion regions are precisely formed.

23/3,AB/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003174969
WPI Acc No: 1981-35519D/198120
Gallium arsenide MOS **FET** - is made by **implanting** **impurity** ions to form relatively **thin** active **layer** in **gate electrode**
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 56032771	A	19810402				198120 B

Priority Applications (No Type Date): JP 79108952 A 19790827

Abstract (Basic): JP 56032771 A

After a masking layer is formed on a gate electrode portion of GaAs substrate, **impurity** ions are **implanted** into the substrate to make a thinner GaAs active **layer** of the gate **electrode** portion than source and drain electrode portions. Source, drain and gate electrodes are bonded to respective regions.

GaAs MOS **FET**'s with high breakdown voltage between drain and gate electrodes are provided because the electric potential at the drain electrode is decreased.

In further detail a masking layer (41) of Al is formed on a gate electrode portion of a semi-insulating GaAs substrate (42) **doped** with Cr. Si ions are **implanted** into the substrate so as to obtain GaAs active layer (43) having the gate portion of 0.2 microns thickness and source and drain regions of 0.4 microns thickness. After removing the masking layer from the substrate surface, source, drain and gate electrodes are formed on the active layer.

23/3,AB/18 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002533941
WPI Acc No: 1980-51965C/198030
Large scale integrated circuit prodn. with mos **fets** - having self aligning connections to source drain zones produced by diffusion or **ion implantation** (NL 10.7.80)
Patent Assignee: AMERICAN MICROSYSTEMS (AMMI-N)
Inventor: BATRA T L
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3000121	A	19800717				198030	B
NL 7908534	A	19800710				198030	
GB 2040564	A	19800828				198035	
FR 2446011	A	19800905				198043	
CA 1131796	A	19820914				198245	
IT 1130200	B	19860611				198746	

Priority Applications (No Type Date): US 791840 A 19790108; US 81287388 A 19810727

Abstract (Basic): DE 3000121 A

The following stages are used in the prodn. of an integrated **semiconductor** device with a no. of **FETs** having self-aligning connections to the source and drain zones and the gate electrodes connected to connecting leads. A **doped semiconductor** substrate of the first conductivity type is used. A limited field **oxide layer** is formed on and/or buried in the substrate, leaving exposed areas of the substrate surface for each **FET**. A relatively **thin gate dielectric layer** is formed on these exposed areas. An electrically **conductive layer** is formed selectively on the **dielectric layer** to give gate **electrodes** of given shape and thickness. A **layer** of **dielectric** material is formed on the side and top of the gate electrode.

Source and drain zones with the opposite conductivity type to the substrate are formed on the remaining exposed areas of the field **oxide layer**. The extent of these zones is determined by the edges of the gate electrodes and hence are self-aligned w.r.t. these edges. A relatively **thin** protective **dielectric layer** is formed over the entire device and then a relatively thick **insulating layer**. Oversize windows are formed in this **layer** above the gate **electrode** and the source and drain zones and the oxide and dielectric material are removed in these areas. Then a pattern of metallic, highly conductive connecting leads is formed, which extends into the windows in this layer from the insulant for the dectric terminals to the source and drain zones and to the gate electrode.

Large scale integration is possible, with an esp. small area per MOS transistor. In spite of this, the source-drain zones of the **FETs** can be produced in the usual way by diffusion or **ion implantation**.

23/3,AB/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

001830948
WPI Acc No: 1977-51943Y/197729
Field effect transistors prodn. - with self-registering connections between gate electrodes and metallic interconnection lines
Patent Assignee: IBM CORP (IBMC)
Number of Countries: 007 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4035198	A	19770712				197729	B
DE 2723374	A	19780105				197803	
JP 53003780	A	19780113				197808	
FR 2357066	A	19780303				197814	
GB 1520718	A	19780809				197832	
CA 1078077	A	19800520				198023	
IT 1115346	B	19860203				198724	

Priority Applications (No Type Date): US 76701442 A 19760630

Abstract (Basic): US 4035198 A

FET is made by (a) providing a **semiconductor** substrate (b) forming field oxide insulation regions to lie between subsequently formed **FETs** (c) forming **thin FET gate insulator layer** (d) depositing **conductive** gate electrode **layer** above **insulator** (e) depositing non-oxidising mask (f) etching **FET** gates and interconnection patterns of gate electrode (g) diffusing or **ion-implanting doped**-Si source and drain regions, self-aligned with the gate electrode edges (h) growing thermal **oxide** partial **insulation layer** over source and drain and sides of gate (i) removing non-oxidising layer (j) depositing an etch stopping layer (k) depositing a thick **insulation layer** (l) opening small holes through **insulation layer** to give access to gate electrode and partial access to source and drain (m) removing etch stopping layer in contact areas (n) etching open the small holes to the source and drain (o) depositing conductive interconnection line pattern to gate electrodes and source and drain regions and (p) forming a connection to the substrate.

Use of etch stopping layer allows use of thick **oxide insulation layer** which provides lower processing temps., due to thick **oxide layer**, metallic interconnections have low capacitive coupling toother elements; polySi gate electrode material may be used as interconnection line material and may cross under metallic lines without making connection to them.

23/3,AB/20 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04090765
SEMICONDUCTOR DEVICE AND MOS **FET**

PUB. NO.: 05-082465 [JP 5082465 A]
PUBLISHED: April 02, 1993 (19930402)
INVENTOR(s): FUNAKI MASANORI
APPLICANT(s): VICTOR CO OF JAPAN LTD [000432] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-271983 [JP 91271983]
FILED: September 24, 1991 (19910924)
JOURNAL: Section: E, Section No. 1407, Vol. 17, No. 415, Pg. 76, August 03, 1993 (19930803)

ABSTRACT

PURPOSE: To control the work function of a **semiconductor** element.

CONSTITUTION: On an n(sup -) substrate 1, a thermal **oxide film** 2 of 1500 angstroms in thickness is formed, on which polycrystalline silicon **thin film** 3 of 3800 angstroms in thickness is formed by a vacuum CVD method. By **implanting** B (boron) as an acceptor and P (phosphorus) as a donar in the polycrystalline silicon **thin film** 3, the same amount of high concentration acceptor and donar are introduced. By performing heat treatment at 850 deg.C for 60 minutes in an N(sub 2) atmosphere, the **implanted impurities** are diffused and activated, and a **semiconductor** device shown by (A) is manufactured. Further, as shown by (B), a gate electrode 3a is formed by etching the polycrystalline silicon **thin film** 3. The **gate electrode** 3a can control the work function between the n(sup +) type and the p(sup +) type, by changing the **implantation** amounts of P and B.

23/3,AB/21 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03331728
MOS-**FET** AND MANUFACTURE THEREOF

PUB. NO.: 02-307228 [JP 2307228 A]
PUBLISHED: December 20, 1990 (19901220)
INVENTOR(s): MINAMI FUYUMI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-129329 [JP 89129329]
FILED: May 23, 1989 (19890523)
JOURNAL: Section: E, Section No. 1042, Vol. 15, No. 98, Pg. 82, March 08, 1991 (19910308)

ABSTRACT

PURPOSE: To reduce a resistance between source, drain and a gate electrode and to improve transistor characteristics by forming the side face shape of an upper half of a polysilicon **layer** of the **gate electrode** in a **tapered** shape extending from its upper part toward its lower part, and forming a high melting point metal layer in the same width as that of the upper part of the polysilicon layer.

CONSTITUTION: In a MOS-PET provided with a gate electrode 4 of a 2-layer structure having a polysilicon layer 6 and a high melting point metal layer 5 covering the upper part on a gate **oxide film** 3 covering an element region, the side shape of the upper part of the layer 6 is formed in a tapered state extending from the upper part toward the lower part, while the layer 5 is formed in the same width as that of the upper part of the layer 6. Thus, with the gate electrode as a mask predetermined **impurity** ions are **implanted** . Then, source and drain of LDD structure in which two **impurity** diffused regions having different junction depths and **impurity** concentrations are continuously formed are composed, and the source and the drain are superposed with the gate electrode.

23/3,AB/22 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03187238
MANUFACTURE OF MOS **FET**

PUB. NO.: 02-162738 [JP 2162738 A]
PUBLISHED: June 22, 1990 (19900622)
INVENTOR(s): YOSHIDA SHINJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-317951 [JP 88317951]
FILED: December 15, 1988 (19881215)
JOURNAL: Section: E, Section No. 976, Vol. 14, No. 421, Pg. 117, September 11, 1990 (19900911)

ABSTRACT

PURPOSE: To contrive a reduction in the film thickness of a gate electrode while a sufficient thickness is secured for the gate electrode to be used as an **ion-implantation** mask by a method wherein the thickness of a poly silicon film to be used as the **film** for the **gate electrode** is made **thinner** than a conventional poly silicon film, while a silicon nitride film is superposed on the poly silicon film to form the gate electrode into a double structure.

CONSTITUTION: A silicon substrate 4 completed a LOCOS process is oxidized to form a gate **oxide film** 6. Then, a poly silicon film 1 to be used as a gate **electrode film** is laminated thinner than a conventional poly silicon film and a nitride film 7 is deposited thereon to make up for the amount of the shortage of a masking effect at the time of **ion-implantation** . Then, after a gate electrode pattern consisting of a photoresist is molded on the film 7, the films 7 and 1 are continuously etched by an RIE method. Then, an **impurity** for a region to be used as a light drain is **ion-implanted** in a self-alignment manner. Then, when an oxidation is performed, the side surfaces only of a gate electrode are oxidized and sidewalls 8 are formed. After this, an **ion-implantation** for forming low-resistance regions 2a and 3b with a deep junction between them is performed and lastly, the film 7 on the gate electrode is removed.

23/3,AB/23 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

03163249
MANUFACTURE OF MIS **SEMICONDUCTOR** DEVICE

PUB. NO.: 02-138749 [JP 2138749 A]
PUBLISHED: May 28, 1990 (19900528)
INVENTOR(s): MIZUTANI KAZUHIRO
MURAO TOSHIAKI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-292604 [JP 88292604]
FILED: November 18, 1988 (19881118)
JOURNAL: Section: E, Section No. 965, Vol. 14, No. 380, Pg. 119, August 16, 1990 (19900816)

ABSTRACT

PURPOSE: To obtain a desired threshold voltage by a method wherein a **gate** electrode is formed **thinly** and even if an **impurity**, which is introduced for forming pocket layers, passes through the gate electrode and changes the profile of the **impurity** concentration in a channel, the **impurity** concentration in the channel is ready-set in advance so as to cancel the amount to correspond to the change.

CONSTITUTION: A poly silicon layer 4 is formed on an n-type well layer 17 with a gate **oxide film** 3, which is formed on its surface, of a MIS-**FET** and an opposite conductivity type first **impurity** is introduced through this layer 4 to form a p(sup -) **impurity** layer 9 for threshold value control use. Then, the layer 4 is patterned to form a gate electrode 5, then, a second **impurity** is introduced to form n(sup +) pocket type **impurity** layers 11 of a high concentration to the concentration of the **layer** 17. Moreover, **insulator** sidewalls 6 are respectively formed on the side surfaces of the electrode 5 and p(sup +) **impurity** layers 12 are formed in such a way that the layers 11 are remained in the interior of the **layer** 17 under the **electrode** 5. At that time, a change of a threshold value, which is generated by the passage of the second **impurity** through the electrode 5, is cancelled and the profile of the **impurity** concentration in the layer 9 is set.

23/3,AB/24 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

02725975
THIN FILM TRANSISTOR

PUB. NO.: 01-023575 [JP 1023575 A]
PUBLISHED: January 26, 1989 (19890126)
INVENTOR(s): KUBOTA YASUSHI
KUDO ATSUSHI
KOBA MASAYOSHI
APPLICANT(s): SHARP CORP [000504] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-179687 [JP 87179687]
FILED: July 17, 1987 (19870717)
JOURNAL: Section: E, Section No. 757, Vol. 13, No. 201, Pg. 155, May 12, 1989 (19890512)

ABSTRACT

PURPOSE: To obtain high efficiency when polycrystalline silicon is hydrogenated, by using a single substance of specific metals or an alloy material of them to form a **gate electrode** in a **thin film** transistor which forms a MISFET.

CONSTITUTION: A gate electrode 5 in in **FET** is formed of a single substance of one species out of M(sub 0), W, Ta, Ti, Pt, Pd, and Cu, or it is formed of an alloy material of them. Namely an active layer part 2 of a polycrystalline silicon **thin film** is formed on a substrate 1, and a silicon **oxide film** 3 is piled on the part 2, and a silicon nitride film 4 is piled on the film 3 to form a gate **insulation film** . In succession, for example, single-substance molybdenum is piled on the film 4, and next it is patterned to form a gate electrode 5, and B ions are **implanted** to form source and drain parts. Annealing is performed to activate the **implanted impurities**. A silicon nitride film 7 is piled and then contact holes 8 and 9 are opened there. After the piling of AlSi, source and drain electrodes 10, 11 are formed. Finally, annealing is performed to make hydrogen in the silicon nitride film diffused in the active **layer**. Accordingly this gate **electrode** can be formed high in hydrogen transmissivity, and so hydro genation efficiency can be upgraded.

23/3,AB/25 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

01611472
MIS TYPE **SEMICONDUCTOR** DEVICE

PUB. NO.: 60-089972 [JP 60089972 A]
PUBLISHED: May 20, 1985 (19850520)
INVENTOR(s): UNO TAKASHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-198592 [JP 83198592]
FILED: October 24, 1983 (19831024)
JOURNAL: Section: E, Section No. 345, Vol. 09, No. 240, Pg. 6, September 26, 1985 (19850926)

ABSTRACT

PURPOSE: To obtain a short channel IG **FET** having small junction capacity by forming a region which has the same conductive type as a **semiconductor** substrate and high **impurity** density more deeply than source and drain regions in a channel region disposed between the source and drain regions formed in the surface layer of the substrate.

CONSTITUTION: A thick **insulator** separating field **insulating film** 8 is formed on the periphery of a **semiconductor** substrate 3, and a **thin gate insulating film** 7 is **coated** on the surface of the substrate 3 surrounded by the film 8. Then, ions are **implanted** through the film 7 to form source and drain regions 2 of different conductive type from the substrate 3, and a region 1 which has the same conductive type as the substrate 3 and high **impurity** density is formed more deeply than the region 2 in the region 4 between the regions 2. At this time the region 1 does not penetrate the source and drain junction due to the fact that the **impurity** density of the region 2 is high. Then, a gate **electrode** 6 is **coated** on the film 7 between the regions 2.

23/3,AB/26 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

01558673
MANUFACTURE OF FIELD EFFECT TRANSISTOR

PUB. NO.: 60-037173 [JP 60037173 A]
PUBLISHED: February 26, 1985 (19850226)
INVENTOR(s): ASAI SHUJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-144785 [JP 83144785]
FILED: August 08, 1983 (19830808)
JOURNAL: Section: E, Section No. 326, Vol. 09, No. 159, Pg. 63, July 04, 1985 (19850704)

ABSTRACT

PURPOSE: To form high concentration N(sup +) type **conductive layers** to be used as a source part and a drain part with high precision, having favorable reproducibility and by selfalignment up to the neighborhood of a gate electrode at a Schottky barrier gate field effect transistor.

CONSTITUTION: A gate pattern 21 and a mask 22 to cover the peripheral part of an **FET** are formed on the plasma nitride film 23 of an N type active layer 5. The surfaces of the patterns 21, 22 thereof are covered with a silicon **oxide film** 24. Then only the amount of thickness of the **oxide film** 24 is removed according to parallel electrode type dry etching to leave the side walls 24 of the **oxide film** on the sides of the Mo gate pattern 21, and Si ions are **implanted** through the plasma nitride film 23 to form high concentration **impurity** layers 6 using the remaining side walls as masks. Then crystallinities of the active layer 5 and the high concentration **conductive layers** 6 are recovered by heat treatment, a silicon **oxide film** 26 is covered thereon as a coating film, and a photo resist film 27 is applied to be dried. Accordingly, the surface of the photo resist film 27 is smoothed, and the photo resist film 27 on the **gate** pattern 21 is **thinned**. The whole surface is etched according to parallel electrode type dry etching to expose the Mo gate pattern 21.

23/3,AB/27 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

01537478
MANUFACTURE OF FIELD EFFECT TRANSISTOR

PUB. NO.: 60-015978 [JP 60015978 A]
PUBLISHED: January 26, 1985 (19850126)
INVENTOR(s): ASAI SHUJI
KOZU HIDEAKI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-124003 [JP 83124003]
FILED: July 07, 1983 (19830707)
JOURNAL: Section: E, Section No. 319, Vol. 09, No. 131, Pg. 4, June 06, 1985 (19850606)

ABSTRACT

PURPOSE: To enable the stable manufacture with good reproductivity of MESFET having food Schottky properties and **FET** properties by a method wherein the gate pattern having vertical walls is connected into an inverted shape as a gate opening on the coating film and heat treatment for recovering the crystal properties is performed while retaining the gate with the vertical walls thereby filling the gate opening with the gate metal again.

CONSTITUTION: An N type operation layer 5 is formed on the high-resistance GaAs substrate 4 and the mask 22 for covering the gate pattern 21 and the periphery of the **FET** is formed. Then the Si ions are **implanted** to form a high- concentration **impurity** layer 6. Subsequently, the substrate is covered with a plasma nitride film 23 and is subjected to the heat treatment in hydrogen to recover the crystal properties of the operation layer 5 and the high-concentration **conductive layer** 6. Next, a photoresist film 24 is spread and dried to be levelled **thinly**. Then, the **gate** pattern 21 is exposed and the photoresist **film** 24 and the **oxide film** 21 are removed to form the opening 25. Next, Al is vapor-deposited over the whole surface to form the Al gate electrode 1. On the **conductive layer** 6, AuGe-Pt is vapor-deposited followed by heat treatment to diffuse AuGe into the **conductive layer** 6 thereby forming the ohmic electrodes 2 and 3 of the source and drain.

23/3,AB/28 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

01155869
ACTIVE MATRIX SUBSTRATE

PUB. NO.: 58-093269 [JP 58093269 A]
PUBLISHED: June 02, 1983 (19830602)
INVENTOR(s): MISAWA TOSHIYUKI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-192120 [JP 81192120]
FILED: November 30, 1981 (19811130)
JOURNAL: Section: E, Section No. 194, Vol. 07, No. 190, Pg. 105, August 19, 1983 (19830819)

ABSTRACT

PURPOSE: To obtain a substrate for a liquid crystal element having good retentivity by accumulating the first polycrystalline Si layer through an oxidized film on a transparent quartz substrate, **doping** an **impurity** on the portion except a channel region, dividing the layer into two sections, and forming electrodes which are made of the second polycrystalline Si on the channel and other regions.

CONSTITUTION: An SiO(sub 2) film 302 is coverd on a transparent quartz substrate 301, and the first polycrystalline Si layer 304 of large area which surround the first polycrystalline Si layer 303 of small area is accumulated on the film 302. Subsequently, a mask of an SiO(sub 2) film 305 is formed only on the layer 303, ions are **implanted** to impart electroconductivity to the film 304 except the film 305, and the polycrystalline layer is divided into a layer 308 which does not include the layer 303 and layers 306, 307 which are disposed at both sides of the layer 303. In this manner, the layer 303 is used as the channel region of an **FET**, the layers 306, 207 are respectively used for source and drain regions, the layer 308 is further used as the **electrode** of a **thin film** capacitor, a **gate electrode** 312 is covered on the layer 303 and a capacitor electrode 313 is coverd on the layer 308 through SiO(sub 2) films 309, 310 with the second multilayer Si.

23/3,AB/29 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

01057073
MANUFACTURE OF **SEMICONDUCTOR** DEVICE

PUB. NO.: 57-207373 [JP 57207373 A]
PUBLISHED: December 20, 1982 (19821220)
INVENTOR(s): NOZAKI TADATOSHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-091830 [JP 8191830]
FILED: June 15, 1981 (19810615)
JOURNAL: Section: E, Section No. 164, Vol. 07, No. 62, Pg. 8, March 15, 1983 (19830315)

ABSTRACT

PURPOSE: To obtain an MOS type **FET** having high threshold voltage by laminating and forming polycrystal Si containing an **impurity** and a silicide **layer** onto a gate **oxide film** with an opening, boring an opening to the silicide layer and thermally treating the silicide layer when source and drain regions are shaped into a **semiconductor** substrate.

CONSTITUTION: A thick field **oxide film32** is formed to the end section of an Si substrate 31, the substrate 31 surrounded by the film 32 is coated with a **thin gate oxide film** 33, and the openings are bored while being made correspond to the source and drain regions. The polycrystal Si film 34 containing P is grown to the whole surface containing the films 32, 33, and the film 34 is coated with the Mo silicide film 35. The film 35 is patterned and only sections which must function as gate electrode wiring and source and drain layer wiring are left, and the films 34 of sections exposed are changed into **oxide films** through heat treatment in an oxidizing atmosphere while the P in the film 34 is diffused and the source and drain regions 36 are shaped. Accordingly, the silicide film 35' on the film 33 is used as a gate **electrode** and the **films** 35'' extending onto the film 32 from the regions 36 as source and drain wiring respectively.

23/3,AB/30 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

00841373
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 56-161673 [JP 56161673 A]
PUBLISHED: December 12, 1981 (19811212)
INVENTOR(s): TSUJIIDE TORU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-064745 [JP 8064745]
FILED: May 16, 1980 (19800516)
JOURNAL: Section: E, Section No. 99, Vol. 06, No. 47, Pg. 43, March 26, 1982 (19820326)

ABSTRACT

PURPOSE: To accelerate the operation of a **FET** by oxidizing a high density-**doped** polysilicon gate, and injecting ions of source and drain with the gate as a mask, thereby reducing the overlap between a gate **electrode** and a diffused **layer**.

CONSTITUTION: After a gate oxidized film 302 is formed on an MOSFET forming region such as a P type Si substrate 30 or the like, a phosphorus-**doped** polysilicon 303 is, for example, accumulated thereon. Then, polysilicon is patterned, the unnecessary part of the gate film is removed, and a thick oxidized film (approximately 3,000 angstroms thick) 304 is formed around the polysilicon **gate** and a **thin** oxidized **film** (approximately 400 angstroms thick) 305 is formed on a substrate 1, for example, by steam oxidation. Thereafter, with the gate 303 and the film 304 as masks As ions are, for example, injected, it is heat treated to form source and drain diffused layer. Thus, it can form a short channel structure with less superposition of the gate **electrode** and the diffused **layer**, thereby improving the performance index of the **FET** and accelerating the operation.

23/3,AB/31 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO

00799866
SEMICONDUCTOR IC DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 56-120166 [JP 56120166 A]
PUBLISHED: September 21, 1981 (19810921)
INVENTOR(s): SHIMIZU SHINJI
KOMORI KAZUHIRO
OSA YASUNOBU
SUGIURA JUN
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-022760 [JP 8022760]
FILED: February 27, 1980 (19800227)
JOURNAL: Section: E, Section No. 87, Vol. 05, No. 198, Pg. 22, December 16, 1981 (19811216)

ABSTRACT

PURPOSE: To obtain EPROM by providing on the same substrate an **FET** memory part having a two-**layer insulation** gate **electrode** and an **FET** part for driving which is a one-**layer insulation** gate **electrode** and is different in thickness of a gate **insulation film**.

CONSTITUTION: In a part of an Si substrate 1 is arranged a memory line 2 of MISFET having electrodes of a floating gate and a control gate and on the periphery thereof are arranged a decoder 3 constituted by **FET** of depression and enhancement type and by high-pressure-resisting **FET** of enhancement type, an input-output circuit 4, etc., while on the peripheral edge thereof is provided a junction pad. In order to manufacture this EPROM device, one and the same substrate is subjected to the first gate oxidation (It(sub 1)) and then removed by etching except for the prescribed part thereof, the gate oxidation is applied again thereto to form a gate oxidized film being different in thickness (Ir(sub 2)) of film, and further **impurity** ions are struck in a part other than the part where a thick film is formed so as to adjust the threshold voltage of the thick-**film gate** and a **thin-film gate**, whereby the density in the lower part of the thick film is made smaller than that in the lower part of the **thin film**. The threshold value of an MOS element for writing-in and reading-out is set at a desired value in this way and thus the EPROM of high degree of integration is obtained.

23/3,AB/32 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

00763677
SEMICONDUCTOR DEVICE

PUB. NO.: 56-083977 [JP 56083977 A]
PUBLISHED: July 08, 1981 (19810708)
INVENTOR(s): TAMEDA MASATO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-161960 [JP 79161960]
FILED: December 13, 1979 (19791213)
JOURNAL: Section: E, Section No. 76, Vol. 05, No. 153, Pg. 1, September 26, 1981 (19810926)

ABSTRACT

PURPOSE: To obtain an Si gate type **FET** in high reliability by a method wherein after an active region is formed in a **semiconductor** by injecting ions through an oxidized **film**, the **film oxide** contaminated by the ions is removed and the region is covered with a new **insulating film**.

CONSTITUTION: A thick field **insulating film** 3 is formed on the periphery of a P type Si substrate 1, a **thin gate insulating film** is provided on the surface of the substrate 1 surrounded by the film 3 and in the center of the **insulating film**, a gate **electrode** 4 made of the polycrystal Si is fitted. Then, with this as a mask, N type **impurity** ions of As and the like are driven in through the gate **insulating film** to form N type drain regions 2, 2', and the surface is applied an etching until the gate **insulating film** is disappeared to remove the ion contaminated **layer**. After then, **film oxide** 3' containing PSG is newly attached to protect the surface and at this time, the content of PSG is prescribed for 3-9mol% and a P type **impurity** diffusion depth 20 in PSG which is reached when the film 3' is attached is made shallower than those of the regions 2 and 2'.

23/3,AB/33 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

00727874
SEMICONDUCTOR DEVICE AND ITS PREPARATION

PUB. NO.: 56-048174 [JP 56048174 A]
PUBLISHED: May 01, 1981 (19810501)
INVENTOR(s): IWAMATSU SEIICHI
APPLICANT(s): CHIYOU LSI GIJUTSU KENKYU KUMIAI [470093] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-123971 [JP 79123971]
FILED: September 28, 1979 (19790928)
JOURNAL: Section: E, Section No. 65, Vol. 05, No. 109, Pg. 50, July 15, 1981 (19810715)

ABSTRACT

PURPOSE: To obtain an **FET** of low wiring resistance and high speed self-matchingly by forming a gate electrode using Al when making an insulated gate type MISFET and then forming source and drain regions by **ion implantation** using the electrode as a mask.

CONSTITUTION: On the periphery of a P type Si substrate 1, a thick field SiO(sub 2) film 4 is formed, and on the surface of the substrate 1 surrounded by the **film** 4, a **thin gate** SiO(sub 2) film 5 is coated, and on the **film**, an Al gate **electrode** 6 is formed with its one end extending onto the film 4. Next, **implanting impurity** ions 7 into the substrate 1 using the electrode as a mask, N type source and drain regions 8 and 9 are formed, and then casting laser beams 10 all over the surface, the regions 8 and 9 are activated. By so doing, annealing of the regions 8 and 9 becomes self-matching since the surface 11 of the electrode 6 reflects the laser beams 10 and desired characteristics can be obtained.

25/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010097661
WPI Acc No: 1994-365374/199445
XRPX Acc No: N94-286113
RESURF lateral transistor breakdown fabrication method, simultaneous with low power **FET** in integrated circuit - using simultaneous threshold voltage adjust **implant** into both RESURF and low power **FET** channel areas, with **thin gate** oxide
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: EFLAND T R; KWON O; MALHI S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5346835	A	19940913	US 92909244	A	19920706	199445	B
			US 9395805	A	19930721		

Priority Applications (No Type Date): US 92909244 A 19920706; US 9395805 A 19930721
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5346835	A		14	H01L-021/266	Cont of application US 92909244

Abstract (Basic): US 5346835 A

The IC RESURF lateral transistor fabrication involves defining two active device areas in a **semiconductor** layer, one for each of the RESURF transistor and a low power **FET**. Oppositely **doped** drift and RESURF channel regions are formed in the RESURF transistor active area, with the channel the same **conductivity** as the **semiconductor layer**. A RESURF transistor source sub-region is formed at the surface, laterally adjacent the channel and spaced from the drift region. A LOCOS oxide is formed on the drift region surface. The RESURF and low-power transistor channels are simultaneously threshold voltage adjust **ion implanted**.

A gate insulator pref. 200angstrom thick, is simultaneously formed over the RESURF channel and the low-power transistor, and a pair of conductive gates are formed over, and insulated from, each respective channel. Source and drain regions separated by the low-power **FET** channel, a RESURF drain conductively connected to the drift region and spaced from the RESURF source and an additional, higher **doped**, RESURF source sub-region are all simultaneously formed, of opposite **conductivity** to the **semiconductor layer**.

USE/ADVANTAGE - E.g. in car power window drive module. Over 40V drain-gate breakdown. Gate oxide formation, threshold voltage adjust **implant** and source-drain **implant** compatible with VLSI transistor formation; 0.80-0.85V threshold voltage **thin gate** LDMOS device; operates on 5V power supply without performance loss, without additional internal circuitry e.g. charge pump for gate drive.

3,4,5/15

25/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04291721
MANUFACTURE OF **SEMICONDUCTOR** DEVICE

PUB. NO.: 05-283421 [JP 5283421 A]
PUBLISHED: October 29, 1993 (19931029)
INVENTOR(s): ISHIZAKA NAOE
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-074921 [JP 9274921]
FILED: March 31, 1992 (19920331)
JOURNAL: Section: E, Section No. 1501, Vol. 18, No. 66, Pg. 20, February 03, 1994 (19940203)

ABSTRACT

PURPOSE: To enable formation with high controllability by a simple process and improve hot carrier resistance, regarding the manufacturing method of an LDD structure MOS **FET** of an overlap type wherein a gate electrode exists also on a low concentration layer.

CONSTITUTION: The surface of a poly silicon layer 23 is coated with positive type chemical amplification resist 24, and patterned by using a process condition that an insoluble layer is formed on the upper layer, thus forming a resist pattern composed of a main body having a width (b) of a gate **electrode** and an insoluble **layer** which protrudes in an eaves type from the upper layer to both sides and has a width (a). By using said pattern as a mask, the poly silicon layer 23 is anisotropically etched until the silicon substrate 21 is exposed, and a **gate** electrode 25 having **thin gate** electrode protrusions 26 on both sides in the gate lengthwise direction is formed. By using said electrode as a mask, **impurity** ions are **implanted** in the whole surface, and a source region and a drain region composed of low concentration layers 27a, 27b and high concentration layers 28a, 28b are formed at the same time.

25/3,AB/3 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

00771172
HIGH-VOLTAGE RESISTING MOS TYPE **SEMICONDUCTOR**

PUB. NO.: 56-091472 [JP 56091472 A]
PUBLISHED: July 24, 1981 (19810724)
INVENTOR(s): SHIRATO TAKEHIDE
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-169044 [JP 79169044]
FILED: December 25, 1979 (19791225)
JOURNAL: Section: E, Section No. 78, Vol. 05, No. 163, Pg. 65, October 20, 1981 (19811020)

ABSTRACT

PURPOSE: To ensure the omission of mask process when low density **impurities** are formed to secure voltage resistance by providing a low density **impurity** region between a source and drain wire electrode on one hand and a gate electrode on the other.

CONSTITUTION: The source layer 6 of an N(sup +) type Si **layer**, the source wiring **electrode** 11 of Al, the drain layer 7 of N(sup +) type Si layer, the drain layer of an N(sup +) type Si **layer**, the drain wiring **electrode** 12 of Al, a gate SiO(sub 2) film 10 and the gate electrode 13 of Al are provided in an **FET** forming region partitioned by a field SiO(sub 2) film 2 on the surface of a P type Si substrate and P(sup +) type channel cutting layer 3 formed thereunder. An N(sup -) type Si layer 5 is formed by P ion injection via a **thin gate** SiO(sub 2) film with self-coordination made using the electrodes and a thick SiO(sub 2) film 10 as mask.

30/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5650209 INSPEC Abstract Number: B9709-2560R-025
Title: N-channel MOS **FET** degradation by source/drain **implantation**
Author(s): Fuse, G.; Shibata, S.; Kato, Y.
Author Affiliation: Matsushita Electron. Corp., Kyoto, Japan
Conference Title: Ion Implantation Technology - 96. Proceedings of the Eleventh International Conference on Ion Implantation Technology (Cat. No.96TH8182) p.642-5
Editor(s): Ishidida, E.; Banerjee, S.; Mehta, S.; Smith, T.C.; Current, M.; Larson, L.; Tasch, A.; Romig, T.
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA xxvii+832 pp.
ISBN: 0 7803 3289 X Material Identity Number: XX96-01370
U.S. Copyright Clearance Center Code: 0 7803 3289 X/97/$10.00
Conference Title: Proceedings of 11th International Conference on Ion Implantation Technology
Conference Date: 16-21 June 1996 Conference Location: Austin, TX, USA
Language: English
Abstract: Degraded N-channel MOSFETs have humps in their Id-Vd characteristics which are usually attributed to arsenic **dopants** in the channel. The arsenic **dopants** in the channel are due to ion channeling through the poly-silicon gate electrodes during As **implantation** of the **source/drain regions** and from direct arsenic **implant** into the **FET** channel regions. Study of this problem has led us to the discovery of a new mechanism. As **implant** and channeling are not the only causes of the hump. Phosphorous atoms in the gate electrode diffuse into the channel region through **thin gate** oxides which are damaged by channeled arsenic ions during source/drain **implant**. The model is verified by thermal wave experiments.
Subfile: B

30/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013318455
WPI Acc No: 2000-490394/200043
XRAM Acc No: C00-147256
XRPX Acc No: N00-363921
Vertical field effect transistor (**FET**) memory device fabrication
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: CHEN S; LIANG M; LIN C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6093606	A	20000725	US 9835049	A	19980305	200043	B

Priority Applications (No Type Date): US 9835049 A 19980305
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6093606	A		13	H01L-021/336	

Abstract (Basic): US 6093606 A
Abstract (Basic):
NOVELTY - Fabrication comprises forming an array of **FET** cells, forming a set of trenches in a **semiconductor** substrate, forming source connections in substrate at bottom of trenches by **doping**, forming threshold **implant** regions in trench sidewalls, forming **doped drain regions** near substrate surface and **doped source regions** in substrate below bottoms of trenches and **source** connection **regions**, forming tunnel oxide layer over substrate, forming **doped** polysilicon **thin** floating **gate** layer over tunnel oxide layer, etching back floating gate layer to form strips, forming interelectrode dielectric layer over strips and tunnel oxide layer, forming blanket thick **doped** polysilicon control gate layer over dielectric layer and patterning.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for: (a) fabrication as above where interelectrode dielectric layer is composed of ONO and spacers are formed next to sidewalls of control gate electrodes; and (b) fabrication as above where (i) **source** connection **implant region** is formed by anisotropic vertical **implant** of N-type phosphorus **dopant** at 1x1014-1x1015 ions/cm2 at an energy of 20-30 keV, (ii) threshold **implant** regions are formed with rotary oblique angular **ion implant** of P-type boron difluoride **dopant** at 5x1014-5x1015 ions/cm2 at an energy of 20-45 keV.

USE - Vertical transistor memory device.

ADVANTAGE - Reduced cell area. ate patterning and planarisation compatible with logic circuit manufacturing process. High drain current available during programming and reading.

DESCRIPTION OF DRAWING(S) - The drawing shows the device above during one of the fabrication steps.

Device (10)
Spacer glass layer (34)
Interelectrode dielectric layer (30)
Control gate electrodes (CG)
Trenches (18)

Tunnel oxide layer (22)
Connect regions (27)
Floating gate strips (FG)
pp; 13 DwgNo 1L,2L/8

30/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013009768
WPI Acc No: 2000-181620/200016
Related WPI Acc No: 1999-069754; 2000-085641; 2000-194837; 2001-624281
XRAM Acc No: C00-056672
XRPX Acc No: N00-134040
Local oxidation of silicon for self aligned **implantation** of submicron transistors uses striped silicon nitride mask as punchthrough oxide mask
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)
Inventor: PEIDOUS I V
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6022768	A	20000208	US 97956970	A	19971023	200016 B
			US 98166396	A	19981005	

Priority Applications (No Type Date): US 97956970 A 19971023; US 98166396 A 19981005
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6022768	A		15	H01L-021/336	Div ex application US 97956970 Div ex patent US 5849613

Abstract (Basic): US 6022768 A
Abstract (Basic):
NOVELTY - Self-aligned sub-micron transistors are formed by a LOCOS method using a striped silicon nitride mask (Wm) to form a punchthrough oxide mask of varying thickness. The nitride stripes are **narrower** over **gate/drain areas** than over **source areas**.

DETAILED DESCRIPTION - A method of making field effect transistors on a **semiconductor** substrate (10) comprises forming a pad oxide layer (12) followed by a deposited silicon nitride oxidation barrier layer (14) which is patterned to leave nitride stripes of decreasing widths (Wm), one for **source areas** and a **narrower** one for **gate** electrode/**drain areas**. The substrate is thermally oxidized and field oxide formed around the stripes, the substrate is laterally oxidized under the stripes to form a punchthrough oxide over the gate/**drain areas** self-aligned to retained pad oxide over sources. Wet etching removes the nitride, device pad oxide is removed, a P-**dopant** shield is **implanted** , punchthrough oxide removed, a gate oxide formed and gate electrodes formed using N+ **doped** polysilicon. Sidewall spacers are formed by anisotropic plasma etching of an insulating layer and N+ **source/drain regions implanted**.

USE - In forming self-aligned sub-micron **FETs** and bipolar transistors for BiFET and BiCMOS circuits and for bipolar power transistors

ADVANTAGE - The bipolar and **FET** are formed simultaneously, minimizing the thermal budget, collector contact resistances and base current are reduced and transistor gain increased. Emitter, base and collector are self-aligned and the number of masking steps is reduced.

DESCRIPTION OF DRAWING(S) - A cross-section of a LOCOS structure is

shown.
Substrate (10)
Pad oxide (12)
Silicon nitride(Wm) Nitride width (14)
Spacing width (Ws)
pp; 15 DwgNo 1/14

30/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011296199
WPI Acc No: 1997-274104/199725
XRPX Acc No: N97-227022
MOS transistor esp. for peripheral LCD driving circuit - has gate electrode wiring passing over highly **doped** channel stop region placed directly beneath thinned section of isolating insulating region
Patent Assignee: CANON KK (CANO)
Inventor: WATANABE T
Number of Countries: 008 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 772245	A2	19970507	EP 96307889	A	19961031	199725	B
JP 9186340	A	19970715	JP 96283800	A	19961025	199738	
KR 97030787	A	19970626	KR 9651518	A	19961101	199828	
TW 371799	A	19991011	TW 96113248	A	19961030	200036	

Priority Applications (No Type Date): JP 96283800 A 19961025; JP 95284924 A 19951101
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 772245	A2	E	14	H01L-029/78	
Designated States (Regional): DE FR GB IT NL					
JP 9186340	A		9	H01L-029/786	
KR 97030787	A			H01L-027/08	
TW 371799	A			H01L-027/14	

Abstract (Basic): EP 772245 A

The **semiconductor** device includes a **FET** surrounded by an isolating insulation layer, and has one or more of the source wiring, drain wiring and the gate wiring extend over a thinned section of the insulation. There is an **impurity** diffusion region directly beneath the thin section of insulation, having a conductivity type different from the **FET source/drain regions** and having a higher **impurity** concentration than the transistor channel. Pref. the **gate** wiring passes over **thinned** insulation, and has a width less than or equal to the twice the lateral diffusion distance of the **impurity** in the highly **doped** region.

The gate wiring is pref. formed of a conductor material different from the gate electrode material, where the wiring passes over the highly **doped** region. The highly **doped** region pref. surrounds the transistor, and operates as a channel stop layer. The thin section of insulation may be formed simultaneously with the gate oxide film e.g. having a thickness in the range 100 to 100 Angstrom . The transistor structure may be repeated in an LCD read/write circuit structure.

ADVANTAGE - Allows reduced **ion implantation** depth for channel stop layer, with less distance between channel stop and **FET source/drain regions**; prevents parasitic bipolar transistor action and current leakage between source/drain electrodes and substrate.

Dwg.0/8

30/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009756709
WPI Acc No: 1994-036560/199405
XRPX Acc No: N94-028441
Field effect transistor fabrication process with short gate length for high frequencies - using dummy gate as **implant** mask for **source** and **drain regions** and **thinning** dummy **gate** for LDD regions **implant** mask, and forming ohmic and gate electrodes
Patent Assignee: SUMITOMO ELECTRIC IND CO (SUME)
Inventor: MATSUZAKI K; NAKAJIMA S; SUMITOMO Y
Number of Countries: 008 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 581305	A2	19940202	EP 93112253	A	19930730	199405	B
CA 2101125	A	19940131	CA 2101125	A	19930722	199416	
JP 6232174	A	19940819	JP 9364104	A	19930323	199438	
EP 581305	A3	19950111	EP 93112253	A	19930730	199538	
JP 3356817	B2	20021216	JP 9364104	A	19930323	200302	

Priority Applications (No Type Date): JP 9364104 A 19930323; JP 92203503 A 19920730; JP 92326812 A 19921207
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 581305	A2	E	22	H01L-021/338	
Designated States (Regional): DE DK FR GB NL SE					
CA 2101125	A			H01L-029/784	
JP 6232174	A		13	H01L-021/338	
EP 581305	A3			H01L-021/338	
JP 3356817	B2		12	H01L-021/338	Previous Publ. patent JP 6232174

Abstract (Basic): EP 581305 A

The **FET** process involves **implanting** ions in a **semiconductor** substrate (1) e.g. a semi-insulating GaAs substrate to form an active layer (3). A dummy gate is then formed on the **semiconductor** substrate and a **dopant** is **implanted** in the substrate with the dummy gate as a mask to form a **doped** layer. The dummy gate configuration is then reduced pref. by partial plasma etching of the dummy gate side surfaces, and a **dopant** is **implanted** in the substrate to form a second **doped** layer (7), pref. the same conductivity as the first **doped** layer.

An insulating film (8) is formed using the reduced dummy gate. Part of the insulating film on the first **doped** layer (6) is removed and ohmic electrodes (10,11) formed in the exposed region. The insulating film is lifted off using the reduced dummy gate and a gate electrode (12) formed in the lifted off region.

USE/ADVANTAGE - LDD structure. Sub 0.5mum gate length, without initial gate formation at this length, avoiding high precision patterning; increased range of gate metal material; prevents increase in source resistance and eliminates short channel effects.

Dwg.8/28

30/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009074359
WPI Acc No: 1992-201778/199225
XRAM Acc No: C92-091771
XRPX Acc No: N92-152707
FET with inverse silicide T-gate structures mfr. - by a silicide process to reduce parasitic resistance but without causing gate to source drain bridging problems
Patent Assignee: AMERICAN TELEPHONE & TELEGRAPH CO (AMTT); AT & T CORP (AMTT); AT & T BELL LAB (AMTT)
Inventor: CHEN M L; CHEN M
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 490535	A2	19920617	EP 91311048	A	19911128	199225	B
JP 4269873	A	19920925	JP 91320835	A	19911205	199245	
US 5290720	A	19940301	US 90624785	A	19901207	199409	
			US 92824756	A	19920117		
			US 9397932	A	19930726		
EP 490535	A3	19940406	EP 91311048	A	19911128	199522	
EP 490535	B1	19960821	EP 91311048	A	19911128	199638	
DE 69121535	E	19960926	DE 621535	A	19911128	199644	
			EP 91311048	A	19911128		

Priority Applications (No Type Date): US 90624785 A 19901207; US 92824756 A 19920117; US 9397932 A 19930726
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 490535	A2	E	4	H01L-029/784	
JP 4269873	A		5	H01L-029/784	
US 5290720	A		5	H01L-021/265	Cont of application US 90624785 Cont of application US 92824756
EP 490535	B1	E	7	H01L-029/772	
Designated States (Regional): DE FR GB IT					
DE 69121535	E			H01L-029/772	Based on patent EP 490535
EP 490535	A3			H01L-029/784	

Abstract (Basic): EP 490535 A
A method for making a new **semiconductor** device comprising, forming a **gate** structure (9) comprising **thin** oxide (11) and polysilicon layer (13), thin oxide being between substrate (1) and said layer, and on the surfaces of this layer; forming **source/drain regions** (25,27) on opposite sides of the gate; this gate being an inverse T-gate made by forming L-shaped spacers (23) on opposite sides of the gate by depositing a silicon layer (17) and a sacrificial layer (19) over the thin oxide and polysilicon, and removing selectively the silicon and sacrificial layers giving the L-shaped spacers.
Dwg.4/4
Abstract (Equivalent): EP 490535 B
A field effect transistor comprising a substrate (1) and disposed thereon a gate structure (9) comprising oxide (11) and polysilicon layers, said oxide layer (9) being between said substrate (1) and said polysilicon (13); L-shaped silicon spacers (23) on opposed sides of

said gate structure (9); an oxide layer (11) between said L-shaped spacers (23) and said gate structure (9); dielectric sidewalls (31) over said L-shaped spacers (23); **source** and **drain regions** (25, 27) on opposed sides of said gate structure (9); and, a silicide region (33).

Dwg.2/4

Abstract (Equivalent): US 5290720 A

The mfr. comprises (a) forming a **gate** structure comprising a **thin** oxide and polysilicon layer and the oxide is between the substrate and polysilicon layer, and the oxide is between the substrate and polysilicon layer and on the surface of the polysilicon, and (b) forming **source/drain regions** on opposed sides of the gate structure by a single **ion implantation** to form lightly and heavily **doped** regions through L-shaped Si spacers and the lightly **doped** regions are formed underneath the spacers. The gate structure is an inverse T-gate made by forming the L-shaped spacers on opposed side of the gate structure by depositing an Si layer and a sacrificial layer over the thin oxide and polysilicon layers, and selectively removing the Si and sacrificial layers.

Pref. the thin oxide is removed from the polysilicon on top of the gate structure and from the **source/drain regions**. Pref. these **areas** are silicided to electrically connect the gate and L-shaped spacer. Si3N4 dielectric sidewall spacers are pref. formed on the L-shaped spacer.

ADVANTAGE - The mfr. is compatible with a self-aligned silicide mfr.

Dwg.4/4

30/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008848543
WPI Acc No: 1991-352560/199148
Related WPI Acc No: 1990-290010
XRAM Acc No: C91-152150
XRPX Acc No: N91-270022

Lightly **doped** drain trench **FET** for ROM and DRAM cells - self-aligned process has improved reliability, electrical breakdown, short channel effects and adjustable threshold voltage

Patent Assignee: IBM CORP (IBMC)
Inventor: DHONG S H; HWANG W

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5021355	A	19910604	US 90513711	A	19900518	199148	B

Priority Applications (No Type Date): US 90513711 A 19900518; US 89355232 A 19890522

Abstract (Basic): US 5021355 A

Prepn. of self-aligned, lightly **doped** drain/source field effect trench transistor for ROM or DRAM cells comprises **implanting dopants** to form a retrograde well region (15) in an epitaxial layer (12) on a **semiconductor** substrate (10), forming oxide isolations (16) on the well and **doping** between them to give first drain junctions (18). A vertical trench is etched into the well and **dopants implanted** into its vertical sides by low-**angle** oblique **ion implantation**. Si3N4 masking layers are formed on the sidewalls and self-aligned and lightly **doped** second **drain** junction **regions** (24) formed on the walls above the nitride, then buried source junction (26) below the trench bottom formed by low-**angle implantation**. Oxide is grown on the recessed oxide regions and trench bottom, the nitride mask removed and **thin gate** oxide grown on the sidewalls, and the trench filled with poly-Si, which also covers the filled trench and recessed oxide to form transfer gate (32) and wordline elements (33).

USE/ADVANTAGE - Transistor is useful for ROM and DRAM cells and has improved electrical breakdown, short-channel effects, and reliability. The threshold voltage of the vertical transistor may be adjusted by oblique **angle ion implantation** or ER **doping**.

Dwg.1/15

30/3,AB/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002214151
WPI Acc No: 1979-13299B/197907
Mfg. MOSFET having reduced contact area - and flat surface so that electrode pattern can be formed without disconnection of the pattern
Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 54004081	A	19790112				197907 B

Priority Applications (No Type Date): JP 7769310 A 19770610

Abstract (Basic): JP 54004081 A

Process comprises (a) forming an oxidn. resisting mask film (e.g. a silicon nitride film) on a p-type silicon substrate, (b) thermally oxidising the exposed silicon substrate to form a thick field oxide film in the silicon substrate, (c) selectively etching the oxidn. resisting mask film to form a mask pattern, (d) selectively etching the exposed silicon substrate to form recesses for forming **source** and **drain regions**, (e) diffusing or **ion implanting** an n-type **impurity** into the recesses of the substrate to form the n-type **source** and **drain regions**, (f) selectively etching away the mask pattern to expose the surface of the substrate for channel region, (g) forming a **thin gate** oxide film on the exposed surface, (h) removing the remaining mask pattern to expose the surface for making contact regions, (i) forming n-type contact **regions** connected with **source** and **drain regions** respectively at the exposed surface, and (j) forming gate, source and drain electrodes.

30/3,AB/9 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05028712
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 07-321312 [JP 7321312 A]
PUBLISHED: December 08, 1995 (19951208)
INVENTOR(s): FUJITA KOICHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-109619 [JP 94109619]
FILED: May 24, 1994 (19940524)

ABSTRACT

PURPOSE: To reduce the capacity between a gate and a source and that between the gate and a drain and to achieve a high-speed operation of an **FET** by deforming an interlayer insulation film so that the opening region on a substrate surface where a dummy gate is eliminated can be reduced and a gate electrode can be formed at that region.

CONSTITUTION: After a source diffusion layer 6a and a drain diffusion layer 6b are formed with a dummy gate electrode as a mask, silicon oxide film 7 where an **impurity** is **doped** is provided, a dummy gate electrode is selectively eliminated and driven by annealing, and then each electrode is formed. The silicon oxide film 7 flows and is deformed at the time of annealing and driving, an open region where the dummy **gate** is formed is **narrowed** and a **gate** electrode 10c is formed here, thus obtaining a **thin gate** electrode 10c which is **narrower** than the dummy **gate** electrode which is used as a mask when forming the **source** diffusion **region** 6b, thus reducing the gate/drain capacity and gate/ source capacity and improving a high-frequency gain.

30/3,AB/10 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04312466
MANUFACTURE OF HIGH BREAKDOWN-STRENGTH MOS TYPE **FET**

PUB. NO.: 05-304166 [JP 5304166 A]
PUBLISHED: November 16, 1993 (19931116)
INVENTOR(s): KOBAYASHI KAZUO
APPLICANT(s): NEW JAPAN RADIO CO LTD [326320] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-166150 [JP 91166150]
FILED: June 12, 1991 (19910612)
JOURNAL: Section: E, Section No. 1512, Vol. 18, No. 105, Pg. 7, February 21, 1994 (19940221)

ABSTRACT

PURPOSE: To obtain a thick oxide film, by which field strength in the vicinity of a drain is reduced and breakdown strength is increased, on the drain side by leaving a taper-etched field oxide film at a position held by a low-**doped drain region** on the **drain** side and a polysilicon gate.

CONSTITUTION: The surface of a silicon substrate 1 is oxidized, opening sections for the diffusion of a channel stop and for the diffusion of a low-**doped** drain are formed, and a channel stop region and a low-**doped drain region** 2a are formed through a diffusion or **ion implantation**. A field oxide film 4 is shaped by a CVD oxide film, the oxide film having a shape having a smooth tapered angle is left on the section on the gate side of the low-**doped drain region** 2a and the oxide film 4 in an element forming region is removed through **taper** etching, a **gate** oxide film 5 is formed, polysilicon is deposited on the gate oxide film 5 and a polysilicon gate 6 is formed. Accordingly, the increase of breakdown strength can be realized without augmenting manhours and having an effect on the state of a low-**doped** drain layer.

30/3,AB/11 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

01417871
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 59-129471 [JP 59129471 A]
PUBLISHED: July 25, 1984 (19840725)
INVENTOR(s): SUGURO KYOICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-003361 [JP 833361]
FILED: January 14, 1983 (19830114)
JOURNAL: Section: E, Section No. 280, Vol. 08, No. 256, Pg. 103, November 22, 1984 (19841122)

ABSTRACT

PURPOSE: To lower the resistance of a gate electrode or an electric wire for an IG-**FET** while improving chemical resistance and oxidation resistance by constituting these gate electrode or electric wire by two layer structure of metallic layers mainly comprising a high melting-point metal-silicon alloy and Al.

CONSTITUTION: A thick field oxide film 2 is formed to the peripheral section of a P type Si substrate 1, a **thin gate** insulating film 3 is formed on the surface of the substrate 1 surrounded by the film 2, and a MoSi(sub 2) film 4 in approximately 2,000 angstroms thickness and a Si(sub 3)N(sub 4) film 5 in approximately 1,000 angstroms thickness are laminated and applied on the whole surface containing these films. The central surface of the laminated films is coated with a mask made of a photo-resist film 6, only a section functioning as a gate electrode is left through reactive ion etching, and other laminated films are removed. The film 5 is removed, N type **impurity** ions are **implanted** into the substrate 1 on both sides of the gate electrode while using the gate electrode as a mask to form **source-drain regions** 7, the **regions** 7 are coated with oxide films 8, an oxide film 9 is also formed on the side surface of the gate electrode, and the surface is coated with an Al film 10.

30/3,AB/12 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

01364874
MANUFACTURE OF INSULATED GATE TYPE FIELD EFFECT **SEMICONDUCTOR** DEVICE

PUB. NO.: 59-076474 [JP 59076474 A]
PUBLISHED: May 01, 1984 (19840501)
INVENTOR(s): YAMAZAKI SHUNPEI
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-188057 [JP 82188057]
FILED: October 25, 1982 (19821025)
JOURNAL: Section: E, Section No. 262, Vol. 08, No. 185, Pg. 135, August 24, 1984 (19840824)

ABSTRACT

PURPOSE: To obtain a desired **FET** at a low cost by a method wherein a **source** and a **drain region** of an IGFET are formed by placing a substrate into an atmosphere wherein a reactive gas containing a III value or a V value **impurity** is turned plasmatic, and prescribing a junction depth and an **impurity** concentration, when they are formed.

CONSTITUTION: A thick field insulator 2 is formed at the peripheral edge of the **semiconductor** substrate 1, a **thin gate** insulator 4 composed of an SiO(sub 2), an Si(sub 3)N(sub 4), etc. is liquid-deposited on the surface of the substrate 1, and a contact hole 5 is opened at a fixed position. Next, the substrate 1 is placed into the atmosphere wherein the reactive gas containing the III value or V value **impurity** is turned plasmatic, and accordingly a **semiconductor** layer 6 is generated over the entire surface. At the same time, the **source** and **drain regions** 9 and 10 of the junction depth of 200 angstroms -0.3.mu.m and the **impurity** concentration at 10(sup 19)/cm(sup 3) or more are formed in the substrate 1 exposed in the hole 5, a gate electrode 7 is provided between the regions 9 and 10 via a gate insulation film 8 by removing the layer 6, and leads 11 and 12 are mounted on the regions 9 and 10.

30/3,AB/13 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

01115477
MANUFACTUE OF **SEMICONDUCTOR** DEVICE

PUB. NO.: 58-052877 [JP 58052877 A]
PUBLISHED: March 29, 1983 (19830329)
INVENTOR(s): SAKAMOTO ISAO
ANZAI NORIO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-150615 [JP 81150615]
FILED: September 25, 1981 (19810925)
JOURNAL: Section: E, Section No. 182, Vol. 07, No. 140, Pg. 19, June 18, 1983 (19830618)

ABSTRACT

PURPOSE: To improve the reliability of products through self-alignment by selectively introducing an **impurity** to one part of the surface of a second conduction type region by utilizing the difference of the thickness of oxidd films and forming a first conduction type region functioning as an upper gate regarding the manufacture of a junction type field-effect transistor J-**FET**.

CONSTITUTION: Boron is deposited in high concentration in order to form a source and a drain while using an Si(sub 3)N(sub 4) film 5 and an HLD film 6 as masks, the HLD film 6 is removed, and B is diffused into a substrate in a high temperature and humid atmosphere and a P(sup +) **source-drain region** 7 is shaped while a section not coated with the Si(sub 3)N(sub 4) film is oxidized through heat treatment at that time and a thick oxide film 8 (film thickness TOX=400.mu.m) is formed. The Si(sub 3)N(sub 4) film 5 is removed through etching, and the ions of the **impurity**, such as P, As or the like are **implanted** in order to shape the upper gate. An N layer 9 functioning as the gate is formed by utilizing the difference of the thickness of the **thin gate** SiO(sub 2) film 4 with 100.mu.m thickness and the thick SiO(sub 2) film 8, and the mutual positions of the source and the upper gate N layer are prescribed through self-alignment using the Si(sub 3)N(sub 4) film.

30/3,AB/14 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

01057075
MANUFACTURE OF **SEMICONDUCTOR** DEVICE

PUB. NO.: 57-207375 [JP 57207375 A]
PUBLISHED: December 20, 1982 (19821220)
INVENTOR(s): NOZAKI TADATOSHI
OKABAYASHI HIDEKAZU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-091832 [JP 8191832]
FILED: June 15, 1981 (19810615)
JOURNAL: Section: E, Section No. 164, Vol. 07, No. 62, Pg. 8, March 15, 1983 (19830315)

ABSTRACT

PURPOSE: To obtain an MOS type **FET** having high threshold voltage by a method wherein a polycrystal Si film not **doped** and a silicide film are laminated and formed to the whole surface containing a gate oxide film with an opening, the silicide film is patterned, **impurity** ions are **implanted** in the polycrystal film exposed between the pattern, and **source** and **drain regions** are shaped through heat treatment while the polycrystal Si is changed into an oxide.

CONSTITUTION: A thick field oxide film 32 is formed to the peripheral section of a P type Si substrate 31, the inside is coated with the **thin gate** oxide film 33, and the predetermined opening is shaped. The polycrystal Si film 34 to which an **impurity** is not **doped** intentionally and the Mo silicide film 35 are laminated and formed to the whole surface containing these films, and the film 35 is patterned and only gate electrode wiring and source and drain layer wiring are left. P Ions are **implanted** in the film 34 sections exposed between these wiring, the ions are diffused through heat treatment, the N type **source** and **drain regions** 36 are shaped while the films 34 on the regions are changed into the oxide 37, and sections between the films 35', 35'' patterned are insulated and isolated.

30/3,AB/15 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

01057074
MANUFACTURE OF **SEMICONDUCTOR** DEVICE

PUB. NO.: 57-207374 [JP 57207374 A]
PUBLISHED: December 20, 1982 (19821220)
INVENTOR(s): NOZAKI TADATOSHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-091831 [JP 8191831]
FILED: June 15, 1981 (19810615)
JOURNAL: Section: E, Section No. 164, Vol. 07, No. 62, Pg. 8, March 15, 1983 (19830315)

ABSTRACT

PURPOSE: To obtain an MOS type **FET** having high reliability through few processes by depositing a silicide and plycrystal Si containing an **impurity** onto a **semiconductor** substrate, diffusing the **impurity** through heat treatment, forming **source** and **drain regions** and using the silicide and the polycrystal Si left as electrode wiring.

CONSTITUTION: A thick field oxide film 22 is shaped to the peripheral section of a P type Si substrate 21, the surface of the substrate 21 surrounded by the film 22 is coated with a **thin gate** oxide film 23, and openings are bored to **source** and gate forming **regions**. The polycrystal Si film 24 containing P and the Mo silicide film 25 are laminated and shaped onto the whole surface containing the films 22, 23, the mask of resist films 26 according to a predetermined pattern are formed, and the films 25 of sections exposed are removed through etching. The thickness of the films 24 exposed between a gate electrode section 25' and source and drain layer sections 25'' is thinned through etching, the films 26 are removed, the P in the films 26 is diffused through heat treatment, the N type **source** and **drain regions** 26 are shaped, and the remaining sections 25', 25'' are each used as the electrode wiring.

30/3,AB/16 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

00859966
MIS FIELD EFFECT **SEMICONDUCTOR** DEVICE

PUB. NO.: 57-010266 [JP 57010266 A]
PUBLISHED: January 19, 1982 (19820119)
INVENTOR(s): SAKURAI JUNJI
MATSUMOTO TAKASHI
MORI HARUHISA
WADA KUNIHIKO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-084884 [JP 8084884]
FILED: June 23, 1980 (19800623)
JOURNAL: Section: E, Section No. 104, Vol. 06, No. 67, Pg. 162, April 28, 1982 (19820428)

ABSTRACT

PURPOSE: To enhance the speed of an SOS type **FET** made in high density by a method wherein an island-shaped **semiconductor** layer being made the center part thereof thinly is formed on an insulating substrate, and a channel **region** and parts of **source** and **drain regions** are provided in the thin part.

CONSTITUTION: A thick island-shaped p type Si layer is formed on the sapphire substrate 11, for example, and recess parts are formed at the channel region 12 and the neighborhood 12A thereof to make the layer to **thinly**. Then after a **gate** film 13, a polycrystalline Si gate 14 are formed, n type **impurities** are **implanted** in high concentration using the gate 14 as a mask. Accordingly capacitance of the junction of **source** and **drain regions** can be reduced, and moreover the resistance values of the **source** and **drain regions** can be reduced because of having the thick n(sup +) type regions 15, 16. Moreover by setting energy of **implanting** ions as deeper than the region 12A having a thin peak position, concentration of the region 12A can be made as low, and withstand voltage thereof can be enhanced.

30/3,AB/17 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

00780174
SEMICONDUCTOR DEVICE

PUB. NO.: 56-100474 [JP 56100474 A]
PUBLISHED: August 12, 1981 (19810812)
INVENTOR(s): YAMAZAKI SHUNPEI
APPLICANT(s): YAMAZAKI SHUNPEI [000000] (An Individual), JP (Japan)
APPL. NO.: 55-003251 [JP 803251]
FILED: January 14, 1980 (19800114)
JOURNAL: Section: E, Section No. 80, Vol. 05, No. 171, Pg. 141, October 30, 1981 (19811030)

ABSTRACT

PURPOSE: To obtain depression-type **FET** having a high-speed of operation by employing an electrode of platinum or an P(sup +) type **semiconductor** when a region is of N type and of aluminum or an N(sup +) type **semiconductor** when the region is of P type on the occasion that the gate electrode is provided on the **semiconductor** region through the intermeidary of an insulating film.

CONSTITUTION: On the periphery of a P(sup -) type Si substrate 1 a thich field oxidized film 7 is formed and to the surface of the substrate surrounded by the film 7 is connected an N(sup -) type layer 2 of which the density of **impurities** is set to be 10(sup 14)- 3X10(sup 16)/cm(sup 3) so that a vacant layer 11 is easy to expand. Next, in the central bottom part of the layer 2 is formed a P type region 10 by injection of ions, and also by injection of ions, around the regions 2 and 10 N(sup +) type of **source region** 5 and **drain region** 6 are provided.
After that, through the intermediary of a very **thin gate** insulating film whose thickness is 2-200 angstroms , a gate electrode 9 of platinum or the P(sup +) type **semiconductor** having a large work function is fitted to the region 2. At this time, when the device is of P channel, as the electrode, aluminum or the N(sup +) type **semiconductor** having a small work function is employed.

30/3,AB/18 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

00683979
INSULATED GATE TYPE FIELD EFFECT TRANSISTOR

PUB. NO.: 56-004279 [JP 56004279 A]
PUBLISHED: January 17, 1981 (19810117)
INVENTOR(s): IWAHASHI HIROSHI
ASANO MASAMICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-080034 [JP 7980034]
FILED: June 25, 1979 (19790625)
JOURNAL: Section: E, Section No. 51, Vol. 05, No. 51, Pg. 167, April 10, 1981 (19810410)

ABSTRACT

PURPOSE: To provide an insulated gate type field effect transistor (IGFET) having sufficiently high charging capacity when used as a load element by forming a region having the same conducting type as the **source** and the **drain regions** and low **impurity** density while disposing the **region** between the **source region** and the **drain region** under a gate electrode.

CONSTITUTION: A central portion as the element forming region of a P-type **semiconductor** substrate 21 is protruded, the thickness of the other portion is reduced, and N-type **drain** and **source regions** 22 and 23 are diffused in the central portion in space each other. Then, **ion** is **implanted** to the surface layer of the substrate 21 except the regions to form a P(sup +)-type channel cut region 28 is formed on the surface layer of the substrate 21, a thick field oxide film 27 is formed thereon, and a **thin gate** oxide film 25 is coated on the regions 22 and 23 surrounded by the film 27. Thereafter, a gate electrode 25 is bridged over the film 27 and is formed at the end on the film 26 as an **FET**. In this configuration an N(sup -)-type region 24 having narrow width W is newly added between the regions 22 and 23 under the electrode 25 to prevent the decrease of the charging capacity.

30/3,AB/19 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

00438981
SEMICONDUCTOR DEVICE

PUB. NO.: 54-090981 [JP 54090981 A]
PUBLISHED: July 19, 1979 (19790719)
INVENTOR(s): HIRAO TAKASHI
OSONE TAKASHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 53-135598 [JP 78135598]
FILED: November 01, 1978 (19781101)
JOURNAL: Section: E, Section No. 139, Vol. 03, No. 113, Pg. 57, September 19, 1979 (19790919)

ABSTRACT

PURPOSE: To establish the device enabling high speed operation at low voltages, by constituting the inverter circuit with the polycrystal Si resistor including **impurity**, Si gate MOSFET, and the resistance lead region having the same degree of resistance as the gate of **FET**, and by taking the polycrystal Si resistor as the load of **FET**.

CONSTITUTION: The field SiO(sub 2) film 2 is coated on the N type Si substrate 1, and the hole 3 is made on the Si gate MOSFET forming region. Next, the **thin gate** SiO(sub 2) film 4 is grown and the gate electrode of **FET** and the polycrystal Si film 5 being the load are deposited on the entire surface of the substrate 1, and it is covered with the SiO(sub 2) film 6. After that, the film 6 is remained as 6' only on the load region, etching is made by taking this as a mask, the polycrystal Si film 3 is left only on the film 4 and the load, and the diffusion windows 7 and 7' are opened. Next, the P(sup +) type **source** and **drain regions** 8 and 8', and the gate electrode 5', and the lead 5'' of resistance region are formed in the windows 7 and 7' by injecting **impurity** , and the high resistance region 9 is produced on the film 5 under the film 6'.

30/3,AB/20 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO

00435192
MIS TYPE **SEMICONDUCTOR** INTERGRATED CIRCUIT AND ITS MANUFACTURE

PUB. NO.: 54-087192 [JP 54087192 A]
PUBLISHED: July 11, 1979 (19790711)
INVENTOR(s): YO KANJI
YAMASHIRO OSAMU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 52-154482 [JP 77154482]
FILED: December 23, 1977 (19771223)
JOURNAL: Section: E, Section No. 137, Vol. 03, No. 110, Pg. 110, September 14, 1979 (19790914)

ABSTRACT

PURPOSE: To establish IC having a plurality of MISFET's having different Vth without using complicated process, by utilizing the difference of threshold voltage through the conduction type, whether P or N, for the polycrystal Si constituting the gate.

CONSTITUTION: The P type well region 3 is formed by diffusion on the N type Si substrate 1 by taking SiO(sub 2) film 2 as a mask and the specified window is opened on the film 2 including the SiO(sub 2) film caused at the same time. Next, **thin gate** SiO(sub 2) film 4 is produced on the exposed surface in the window and the polycrystal Si gate 5 is coated not including **impurity** is coated on it. After that, **FET**'s 3, 4 formed in the region 3 and **FET**'s 1, 2 formed in the substrate 1 are covered with the photo resist film 6 while restricting the area, forming the P type **source** and **drain region** of P channel **FET**'s 1 and 2 by diffusion. Simultaneously, the gate 5 of **FET**'s 1, 4 is converted into P type. After that, the resist film 6 is renewed and the N type **source** and **drain region** of the N channel **FET**'s 3, 4 is formed by diffusion, and simultaneously, the gate 5 of **FET2** is converted into N type.